Advanced Design System 2011.01

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EDGE Design Library

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About EDGE Design Library

EDGE (enhanced data rates for GSM evolution) is part of ETSI's strategy for GSM toward third-generation wideband multimedia services. EDGE uses 8PSK modulation and new channel coding schemes to enable wireless multimedia IP-based data services and applications at speeds of 384 kbps with a bit-rate of 48 kbps and up to 69.2 kbps per timeslot.

EDGE uses existing GSM radio bands, the same time division multiple access frame structure, logic channel, and 200 kHz carrier bandwidth as today's GSM networks. This allows existing cell plans to remain intact. EDGE requires relatively small changes to GSM network hardware and software.

The EDGE radio interface is designed to work in typical GSM radio environments such as rural area (RA), typical urban (TU), and indoor environments. While EDGE will also work in hilly terrain (HT) environments, the focus is on channels with a lower delay spread than HT, as specified in GSM05.05.

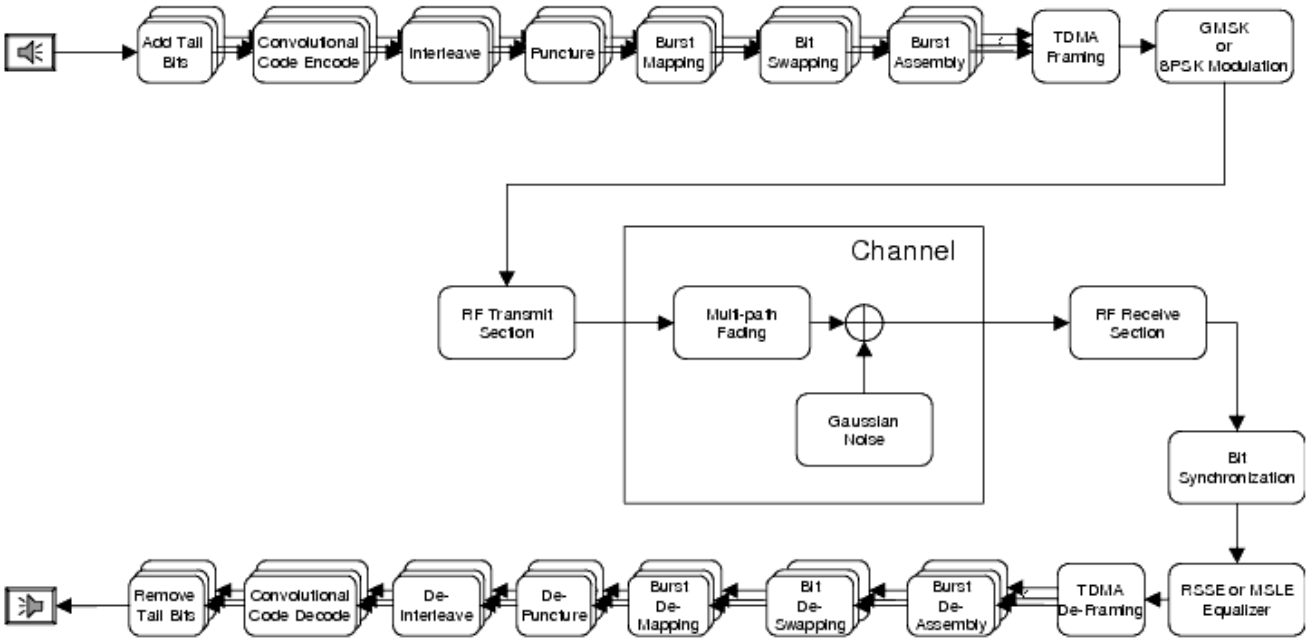
EDGE accommodates E-GPRS (enhanced general packet radio services), T-ECSD (transparent enhanced circuit switched data) and NT-ECSD (non-transparent enhanced circuit switched data).

E-GPRS provides a range of bearer capabilities that depend on environment and user speed. Peak rates are listed in the following table. In addition to peak data rates, the average throughput and area where 384 kbps can be achieved are important measurement parameters. Radio interface optimization provides maximum coverage and availability.

EGPRS Peak Rates

	Indoor, Low-Range Outdoor 384 kbps (48 kbps per timeslot)	**Urban, Suburban Outdoor 384 kbps (48 kbps per timeslot)**	**Rural Outdoor 144 kbps (18 kbps per timeslot)**
Speed	up to 10 km per hour	up to 100 km per hour	up to 250 km per hour
Propagation conditions	Indoor, TU3	TU50 HT100	900MHz: RA250 1800/1900MHz: RA130 HT100

The Agilent EEsof EDGE Design Library includes more than 100 behavioral models and subnetworks that are focused on the simulation of the physical layer supporting E-GPRS services. The physical-layer architecture of the EDGE radio interface is shown in the following figure.



EDGE Physical Layer

Built-in subnetworks speed system construction, such as 8PSK modulation, synchronization, and equalization. Implemented according to ETSI EDGE specifications, these models and subnetworks are organized in component libraries according to function.

- Channel coding includes convolutional code, cyclic code, and Reed-Solomon code encoding and decoding, as well as splitters, combiners, interleavers and de-interleavers, puncturing and de-puncturing models. With these models, 36 subnetworks of encoders and decoders for all uplink and downlink modulation and coding schemes (MCS1 to MCS9) are built in.
- Equalization includes a de-rotator, splitter (splits one burst into two specific frames for bi-directional equalization), combiner (combines the two input frames into one burst after bi-directional equalization), channel estimator, matched filter, and Viterbi algorithm processor.
- Framing includes models and subnetworks that implement construction and disassembly of bursts and TDMA frames.
- Measurement includes models for EVM, BER, FER, and average signal power measurements, non-linear power amplifier, and EDGE signal generation.
- Modem includes pulse shaping filter, receive filter, and phase rotation. An 8PSK modulator is built using these models.
- Synchronization includes training bit generation, phase recovery, and down-sampler.

Agilent Instrument Compatibility

This EDGE design library is compatible with Agilent E443xB ESG-D Series Digital RF Signal Generator.

This EDGE design library is also compatible with Agilent E4406A VSA Series Transmitter Tester and Agilent PSA Series High-Performance Spectrum Analyzer.

The following table shows more information of instrument models, Firmware revisions, and options.

Agilent Instrument Compatibility Information

EDGE Design Library	ESG Models	VSA Models
SpecVersion=8.3.0-1999	E443xB, Firmware Revision B.03.50 Option 202 - "Real-time EDGE" Personality	E4406A, Firmware Revision A.04.21 Option 202 - "EDGE with GSM" Measurement Personality PSA, Firmware Revieion A.02.04 Option 202 - "GSM with EDGE" Measurement Personality

For more information about Agilent ESG Series of Digital and Analog RF Signal Generator and Options, please visit
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For more information about Agilent PSA Series Spectrum Analyzer and Options, please visit
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Channel Coding

There are nine modulation and coding schemes. E-GPRS supports both a pure link adaptation (LA) mode and a combined link adaptation and incremental redundancy (IR) mode. The LA mode is achieved by initially transmitting data using a specified modulation and coding scheme (MCS) based on current link quality. The IR mode is fully supported by the rate-compatible punctured convolutional (RCPC) codes.

Coding schemes differ in bit rate but use the same mother code. Bit rates are achieved by using a different puncturing scheme for each MCS to achieve RCPC codes. Coding parameters for E-GPRS coding schemes are listed in the following table.

The rate 1/3 convolutional coding scheme is used for all MCSs. The last six bits of each bit block delivered to the encoder are tail bits and equal to 0. The polynomials are:

- $G4 = 1 + D^2 + D^3 + D^5 + D^6$ (from GSM 05.03, version 8.5.0, Release 1999)
- $G7 = 1 + D + D^2 + D^3 + D^6$ (from GSM 05.03, version 8.5.0, Release 1999)
- $G5 = 1 + D + D^4 + D^6$ (from GSM 05.03, version 8.5.0, Release 1999)

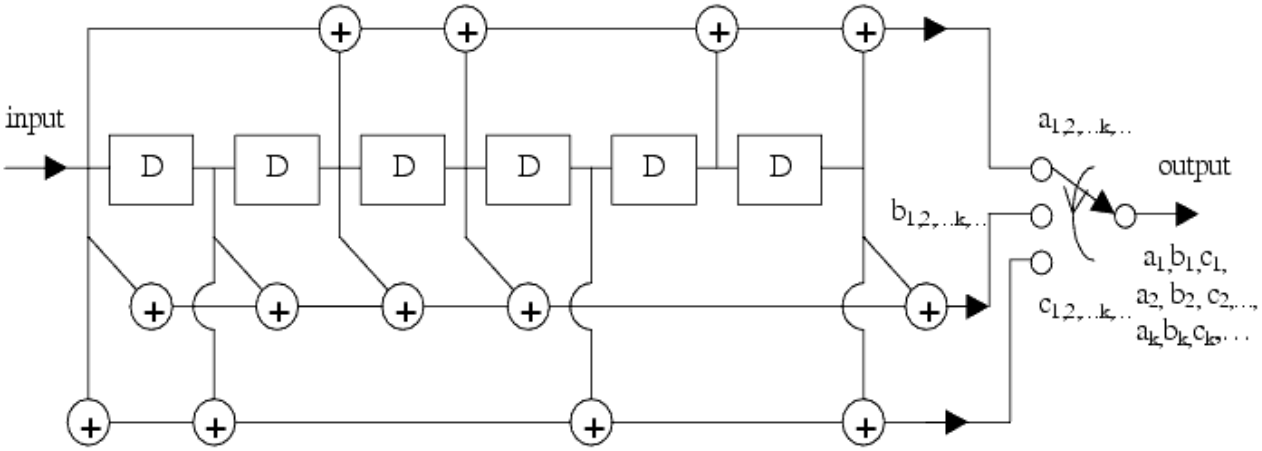
The Viterbi algorithm is used to decode the convolutional code, achieving maximum likelihood sequence decoding. The states and trellis are determined by the constrained length and generator polynomials listed above.

The convolutional encoder schematic is illustrated in the following figure.

Since the data block length of each MCS differs, interleaving is carried out over different data lengths, and over different numbers of bursts. Headers and data are interleaved together in MCS1-4 and interleaved separately in MCS5-9.

E-GPRS Coding Parameters

Scheme	Code Rate	Header Code Rate	Modulation	RLC Blocks per Radio Block (20ms)	Raw Data Within One Radio Block	Family	BCS	Tail Payload	HCS	Data Ratekbps
MCS9	1.0	0.36	8PSK	2	2x592	A	2x12	2x6	8	59.2
MCS8	0.92	0.36		2	2x544	A				54.4
MCS7	0.76	0.36		2	2x448	B				44.8
MCS6	0.49	1/3		1	592544+48	A	12	6		29.627.2
MCS5	0.37	1/3		1	448	B				22.4
MCS4	1.0	0.53	GMSK	1	352	C				17.6
MCS3	0.80	0.53		1	296272+24	A				14.813.6
MCS2	0.66	0.53		1	224	B				11.2
MCS1	0.53	0.53		1	176	C				8.8



Convolutional Code Encoder Schematic

Framing and Deframing

Framing and deframing models are used in EDGE multiplexing and multiple access on the radio path. Physical channels of the radio sub-system, required to support the logical channels according to GSM 05.02, are defined. Included are bursts, time slots, TDMA frames, and multi-frame assembly and disassembly.

EDGE burst structures, time slots, and TDMA frames are the same as those defined in GSM 05.02. EDGE also uses the same number of symbols in each part of the burst.

Multiple Access and Channel Structure

Since radio spectrum is a limited resource shared by all users, bandwidth is divided among as many users as possible. EDGE and GSM use a combination of time- and frequency-division multiple access (TDMA and FDMA).

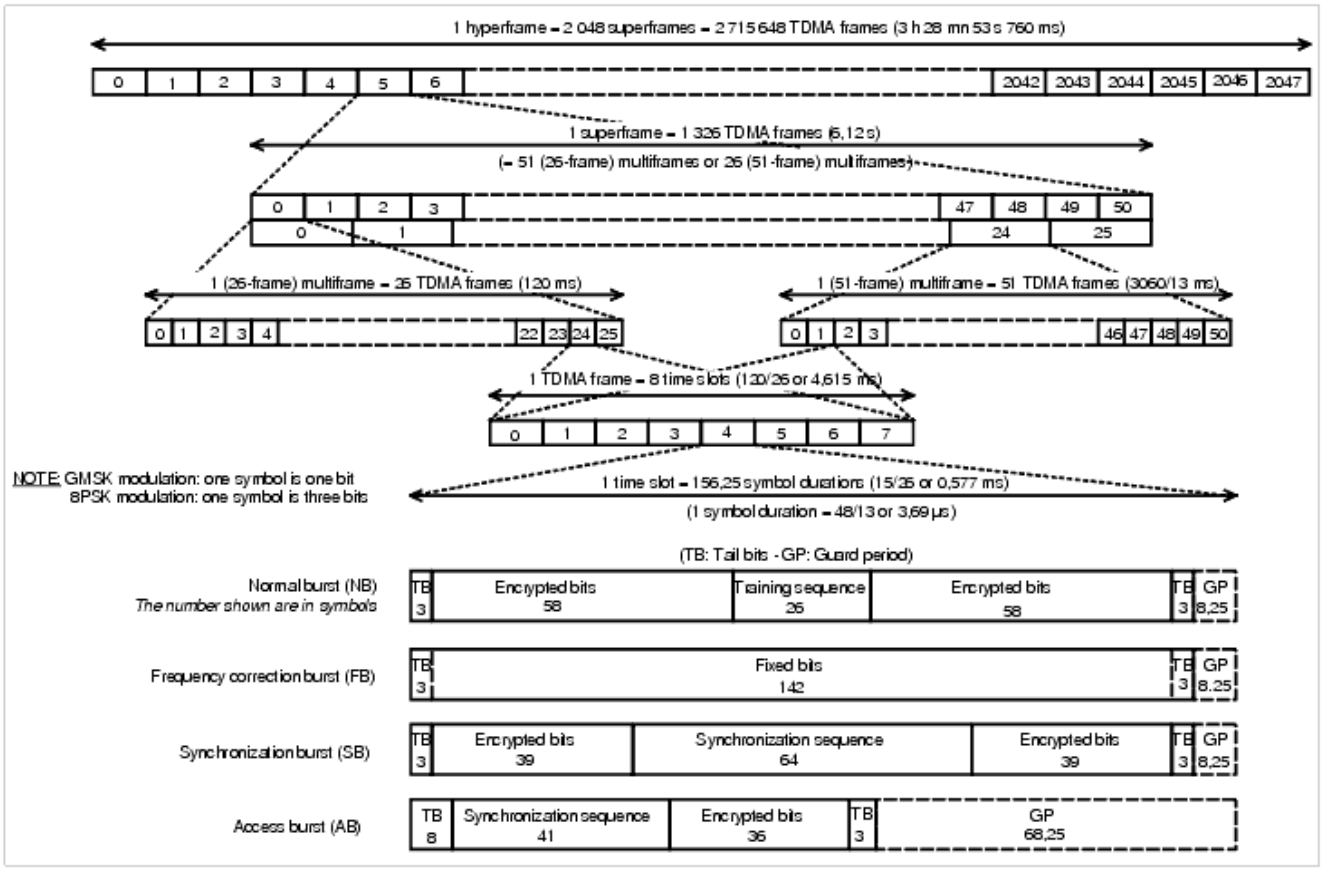
FDMA involves the division by frequency of the (maximum) 25 MHz bandwidth into 124 carrier frequencies spaced 200 kHz apart. One or more carrier frequencies is assigned to each base station. Each carrier frequency is then divided in time, using a TDMA scheme. The fundamental unit of time in the TDMA scheme, a burst period, lasts 15/26 msec (or approximately 0.577 msec). Eight burst periods are grouped in a TDMA frame (120/26 msec, or approximately 4.615 msec).

Burst Structure

Five types of bursts are used for EDGE transmission: normal, frequency correction, synchronization, access, and dummy. There are two models for each burst, one for construction, one for disassembly.

Bursts have a total length of 156.25 symbols and only differ in structure. The normal burst is used to carry data and most signaling; it is made up of two 57-symbol information bits, a 26-symbol training sequence used for equalization, one stealing symbol for each information block (used for FACCH), three tail symbols at each end, and an 8.25-symbol guard sequence. The 156.25 symbols are transmitted in 0.577 msec, giving a gross bit rate of 270.833 kilosymbols per second.

The following figure illustrates the relationship of time frames, time slots and bursts. The number of symbols is the same for 8PSK and GMSK modulation; each 8PSK modulated symbol corresponds to 3 bits while each GMSK modulated symbol corresponds to 1 bit. In 8PSK modulation, each pre-defined bit (training sequence, fixed, synchronization sequence, and tail) is transferred into 3 bits by mapping 0 to 001 and 1 to 111.



Time Frames, Time Slots and Bursts

Modem

In EDGE systems, GMSK and a modified 8PSK modulation schemes are combined with different coding schemes to form nine modulation and coding schemes (MCS) to implement link adaptation (refer to the table of E-GPRS Coding Parameters).

8PSK Modulation

8PSK linear modulation provides high data rates and high spectral efficiency with moderate implementation complexity. In 8PSK modulation, each symbol corresponds to each of the three consecutive bits and is Gray-mapped onto one point on the I/Q axis. The modulation scheme can be expressed as the following equation:

$$S(t) = \sum_{k=0}^{\infty} e^{jk\theta} b_k h(t - kT)$$

where θ is the continuous angle rotation step and is set to be $\frac{3}{8}\pi$

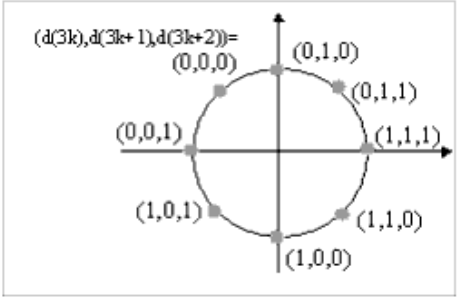
T is the symbol duration, which equals the bit period of GSM, 1/T=1625/6 kilosymbols per second
h(t) is the impulse response of the pulse-shaping filter and is defined to be the first function C0(t) in linearized GMSK modulation
b _k _ is the symbol value taken from the set

$$\left\{ e^{jm\frac{\pi}{4}}, \quad m = 0, \ldots, 7 \right\}$$

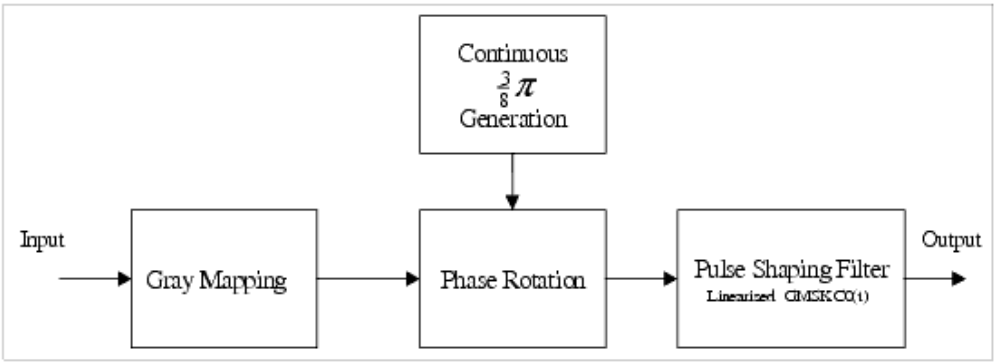
which is Gray-mapped from the three consecutive bits according to the first of the following two figures.

The 8PSK modulation block diagram is shown in the second of the following two figures.

For demodulation of 8PSK signal over fading channel, maximum-likelihood sequence estimation (MLSE) or reduced-state sequence estimation (RSSE) is used.



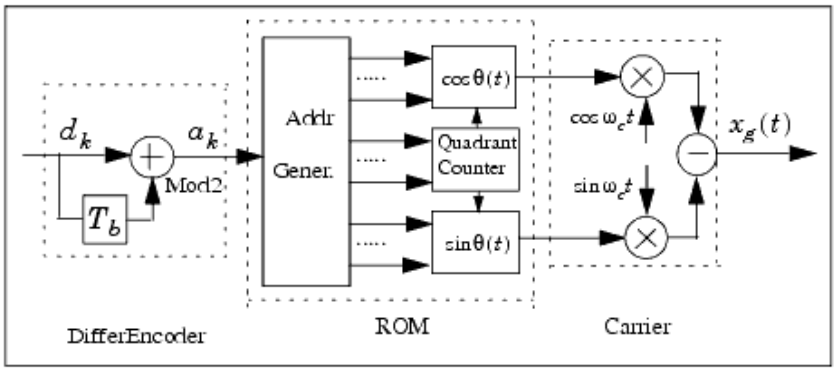
8PSK Modulation Constellation



8PSK Modulation Functional Block Diagram

GMSK Modulation

The GMSK modulation scheme is the same as that used in GSM: BT_b =0.3, and rate=270.833 kilosymbols per second. All models and subnetworks are from the GSM Design Library. The GMSK modulator block diagram is shown in the following figure.



GMSK Modulator Block Diagram

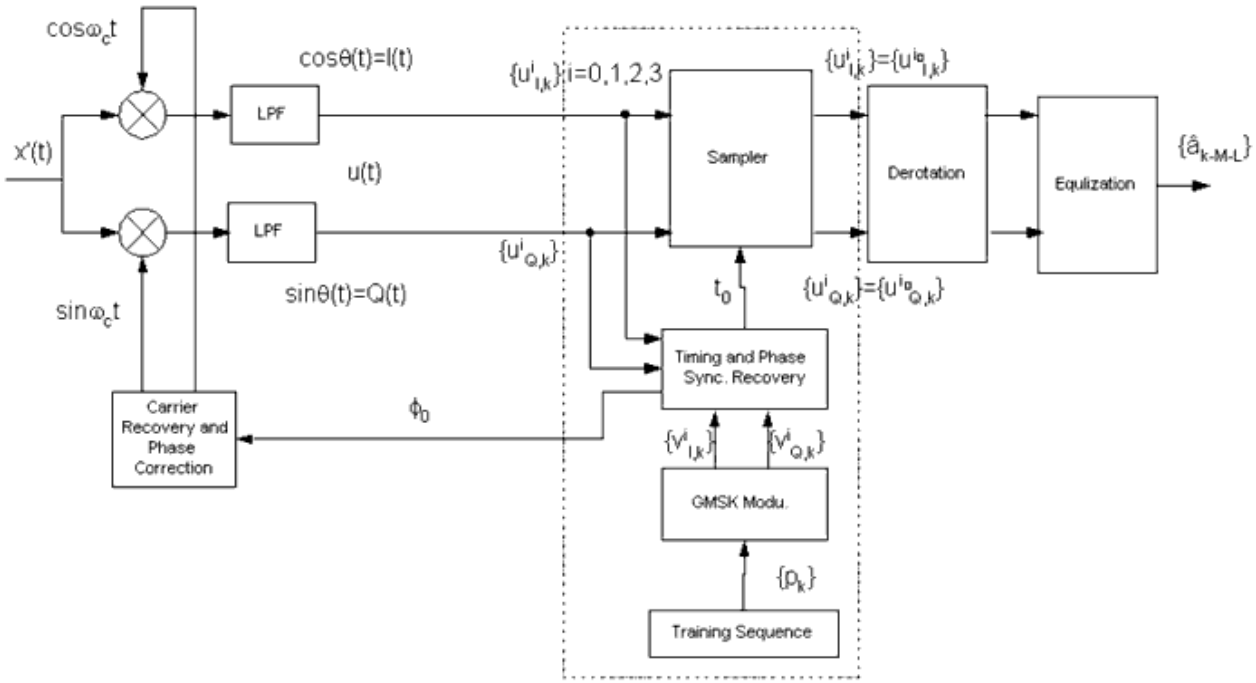
Synchronization

Bit synchronization is carried out before equalization of the EDGE receiver. In a normal burst, eight training sequences are defined with good cross-correlation properties in order to reduce the effects of interference among transmitters operating at the same frequency. All mobiles in a particular cell share the same training sequence (selected with training sequence code parameter TSC). Only the central 16 symbols of the 26-symbol training sequence are selected for correlation properties, because the first and last five symbols are used for the time delay of the channel impulse response and the time-jitter of the received signal burst.

After symbol timing is implemented, one of the sample sequences made up of one sample per symbol will be determined, and the 0.25-symbol from the 156.25 symbols of one burst will be cut. The output of this part will be 156 symbols with one sample per symbol.

The following figure shows the implementation of GSM bit synchronization; here the reference training sequence $\{P_k\}$ is GMSK modulated. The same structure is used for

EDGE bit synchronization, except that the local training sequence can also be 8PSK-modulated according to the modulation type of the input signal.



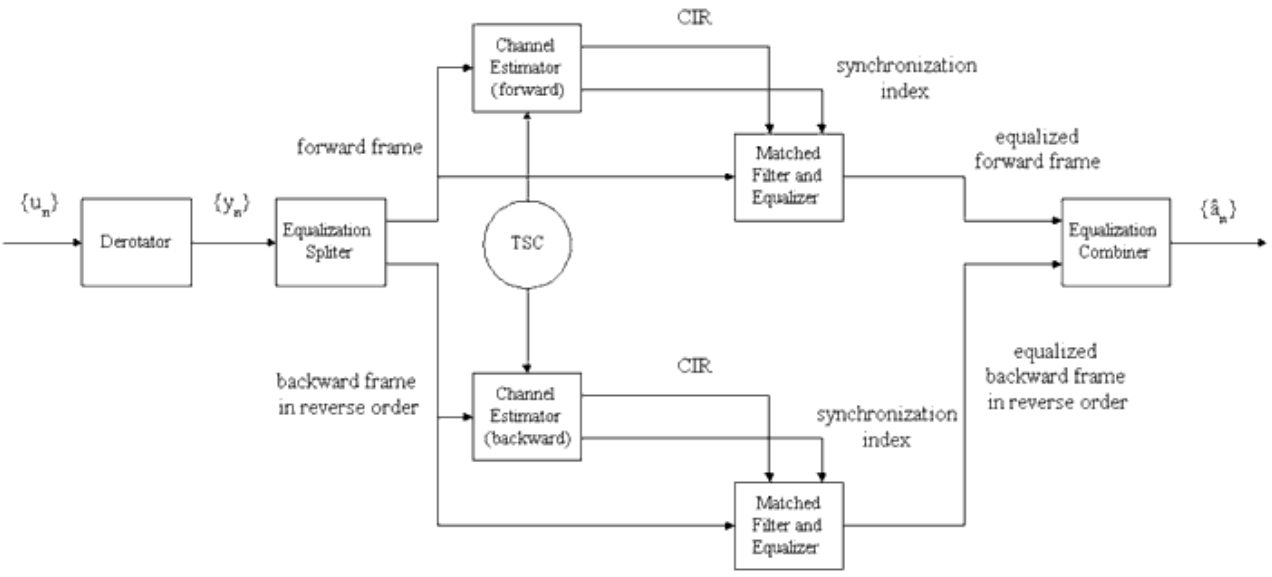
GSM Bit Synchronization

Equalization

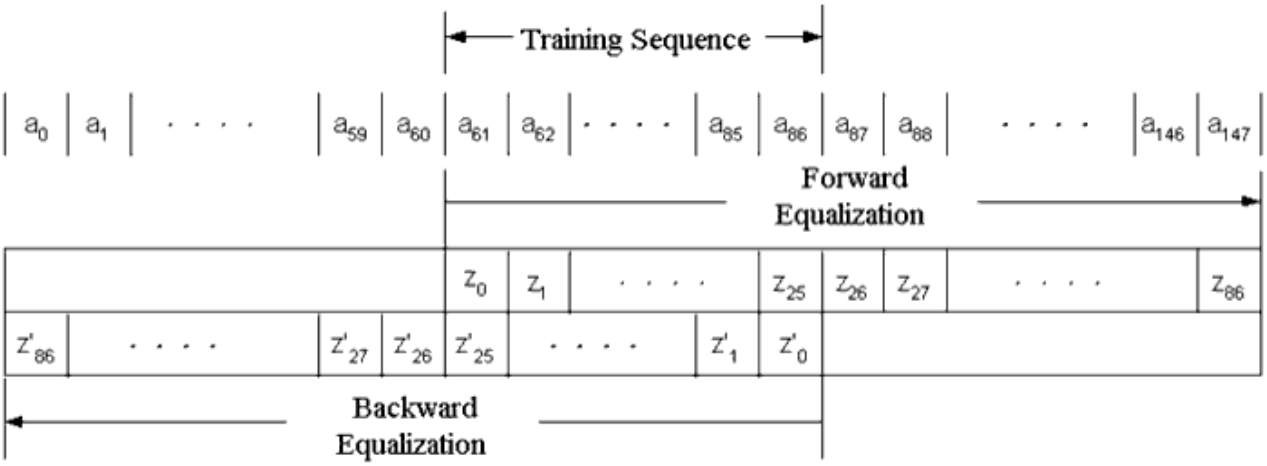
An equalizer is used in the receiver that cancels the inter-symbol interference (ISI) introduced by modulation and channel spreading. For 8PSK-modulated signals, the reduced-state sequence estimation (RSSE) is used to implement the equalizer. For GMSK-modulated signals, maximum likelihood sequence estimation (MLSE), implemented with Viterbi algorithm, is the optimum equalization algorithm.

The bit-synchronized signal is de-rotated to neutralize the continuous $\frac{3}{8}\pi$ phase rotation introduced by 8PSK modulation. The phase de-rotated burst is then split into two sub-frames for bi-directional equalization. The signal of each sub-frame is fed into a channel estimation model, which estimates the channel impulse response in each burst. Assisted by the training sequence and the channel estimates, each sub-frame is equalized with the Viterbi algorithm. The two equalized sub-frames are then combined into one burst. Before equalization, a matched filter is used to obtain the signal with maximum signal-to-noise ratio.

The first of the following two figures shows the equalization receiver block diagram. The second figure illustrates sub-frame splitting for bi-directional equalization.



Viterbi Adaptive Receiver Block Diagram



Bidirectional Equalization on Normal Burst

Glossary of Terms

ACPR	adjacent channel power ratio
AWGN	additive white Gaussian noise
BER	bit error rate
BLER	block error rate
bps	bits per second
BSIC	base station identity code
CIR	channel impulse response
codec	coder and decoder
CRC	cyclic redundancy code
E-GPRS	enhanced general packet radio services
EDGE	enhanced data rates for GSM evolution
EVM	error vector magnitude
FACCH	fast associated control channel
FER	frame error rate
GMSK	Gaussian minimum shift keying
GSM	global system for mobile communications
ISI	inter-symbol interference
K	constraint length
LAR	log-area ratio
LPC	linear predictive coding
LSB	least significant bit
MCS	modulation and coding scheme
MLSE	maximum-likelihood sequence estimation
MS	mobile station
MSB	most significant bit
NT-ECSD	non-transparent enhanced circuit switched data
NRZ	non-return-to-zero
OQPSK	offset quadrature phase shift keying
PDTCH	packet data traffic channel
PLMN	public land mobile network
QPSK	quadrature phase shift keying
RACH	random access channel
RSSE	reduced-state sequence estimation
SACCH	slow associated control channel
SCH	synchronization channel
SDCCH	stand-alone dedicated control channel
SER	symbol error rate
SINR	signal-to-interference noise ratio
SIR	signal-to-interference ratio
T-ECSD	transparent enhanced circuit switched data
TCH/FS	traffic channel/full-rate speech

References

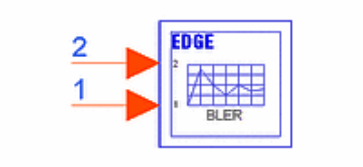
1. D. M. Redl, An Introduction to GSM, Artech House Publishers, Boston.
2. GSM Recommendation 03.03, Numbering, addressing and identification, version 3.5.1, March 1992.
3. GSM Recommendation 04.06, Mobile Station - Base Station System (MS - BSS) interface Data Link (DL) layer specification, version 3.5.1, March 1992.
4. GSM Recommendation 05.01, Physical Layer on the Radio Path General Descriptions, version 3.5.1, March 1992.
5. GSM Recommendation 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
6. GSM Recommendation 05.03, Channel Coding, version 3.5.1, March 1992.
7. GSM 05.03, *Channel Coding* , version 8.5.0, Release 1999.
8. GSM Recommendation 05.04, Modulation, version 3.5.1, March 1992.
9. GSM Recommendation 05.05, Radio Transmission and Reception, version 3.5.1, March 1992.
10. GSM Recommendation 05.10, Radio Subsystem Synchronization, version 3.5.1, March 1992.
11. GSM Recommendation 06.01, Full Rate Speech Processing Functions, version 3.5.1, March 1992.
12. GSM Recommendation 06.10, Full Rate Speech Transcoding, version 3.5.1, March 1992.
13. S. Lin, D. J. Costello, JR., ERROR CONTROL CODING Fundamentals and Applications, Prentice Hall, Englewwood Cliffs, NJ, 1983.
14. J. E. Meggit, "Error Correcting Codes and Their Implementation", IRE Trans. Inf. Theory, IT-7, October 1961, pp. 232-244.
15. *P. Q. Hua, L. W. Dong, H. Y. Hong, "GSM* System GMSK Modulator (in Chinese)", Journal of Beijing University of Posts and Telecommunications, Vol.17, No.4, Dec., 1994, pp.20-25.
16. P. Q. Hua, G. Yong, L. W. Dong, " *Synchronization Design Theory Of Demodulation For Digital Land Mobile Radio System* (in Chinese)", Journal of Beijing University of Posts and Telecommunications, Vol.18, No.2, Jun., 1995, pp.14-21.
17. G. D'Aria, L. Stola, and V. Zingarelli, " *Modeling and simulation of the propagation characteristics of the 900MHz narrowband-TDMA CEPT/GSM mobile radio"* , in Proc. 39th IEEE Veh. Technol. Conf., San Francisco, CA, April 29-May 3, 1989, pp. 631-639
18. G. D'Aria, F. Muratore, " *Simulation and Performance of the Pan-European Land Mobile Radio System* ", *IEEE Trans. on Vehicular Technology* , Vol. 41, No.2, May 1992
19. G. Ungerboeck, " *Adaptive maximum-likelihood receiver for carrier-modulated data-transmission system"* , IEEE Trans. Commun., vol. COM-22, May 1974, pp. 624-636.
20. R. D'Avella, L. Moreno, M. Sant'Agostion, " *An adaptive MLSE receiver for TDMA digital mobile radio* ," IEEE Jour. on SAC, vol. 7, NO. 1, Jan 1989, pp. 122-129.
21. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.
22. ETSI TDOC SMG2 EDGE 278/99, EGPRS Channel Coding, Paris, France, August 24-27, 1999.
23. E.R. Berlekamp, Algebraic Coding Theory, McGraw-Hill, New York, 1968.
24. Tdoc SMG2 EDGE 2E99-403, New Training Sequences for Access Burst due to EGPRS, August 24 -27, 1999.
25. ETSI Tdoc SMG2 WPB 108/98, Ericsson, EDGE Evaluation of 8-PSK.
26. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999.
27. ETSI TDOC SMG2 EDGE 2E99-017, Reference Models for Nonlinear Amplifiers and Phase Noise for Evaluation of EDGE Radio Performance, Toulouse, France, March 2-4,

September 1999.
28. ETSI SMG2 WS #11, Tdoc SMG2 2e99-459, A New Measurement Filter for EDGE, Austin, Texas, October 18-22, 1999.
29. Pierre A. Laurent, Exact and Approximate Construction of Digital Phase Modulations by Superposition of Amplitude Modulated Pulses (AMP), IEEE Trans. Commun., vol. COM-34, NO. 2, pp. 150-160, Feb. 1986.
30. John G. Proakis, Digital Communications, Third Edition, McGraw-Hill, Inc., p 557.
31. Cao Zhigang, Qian Yasheng, Theories of Modern Communications, (in chinese), Publishing House of TsingHua University, pp 215-219.

Base Station Test and Verification Components

- *EDGE BLER* (edge)
- *EDGE BTS MCS5 Receiver* (edge)
- *EDGE BTS MCS6 Receiver* (edge)
- *EDGE BTS MCS7 Receiver* (edge)
- *EDGE BTS MCS8 Receiver* (edge)
- *EDGE BTS MCS9 Receiver* (edge)
- *EDGE MultipathUp* (edge)
- *EDGE Pwr Measure* (edge)
- *EDGE Pwr vs Time* (edge)

EDGE_BLER



Description Block error rate performance measurement
Library EDGE, BTS Test and Verification
Class SDFEDGE_BLER

Parameters

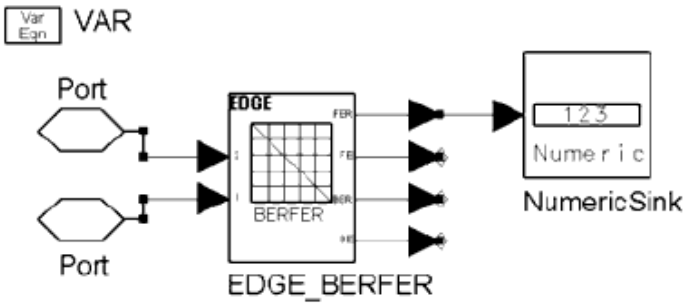
Name	Description	Default	Sym	Type	Range
Start	frame from which measurement starts	0.0	N	int	[0, ∞)
Stop	frame at which measurement stops	100.0		int	[N, ∞)
BlockLength	number of bits in a block	1		int	[1, ∞)
RecordType	type of result recording: Final Value, From Start	Final Value		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	in1	input of the expected sequence or estimated sequence	anytype
2	in2	input of the expected sequence or estimated sequence	anytype

Notes/Equations

1. This subnetwork is used to measure the block error rate for EDGE.
   The schematic for the subnetwork is shown in the following figure. It consists of EDGE_BERFER, NumericSink, and two TkShowValues.



EDGE_BLER Schematic

EDGE_BTS_MCS5_Receiver

Description EDGE BTS MCS5 receiver
Library EDGE, BTS Test and Verification
Class SDFEDGE_BTS_MCS5_Receiver

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_Measured	time slot measured	0		int	[0, 7]
TSC	training sequence code	0		int	[0, 7]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†

† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$, Ji is the number of states on stage i, $1 \le i \le L$

Pin Inputs

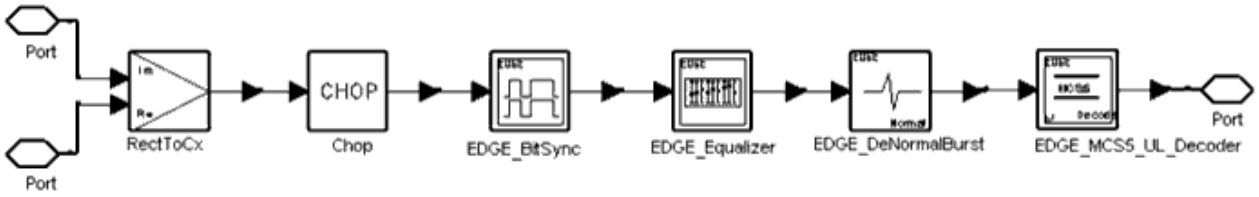
Pin	Name	Description	Signal Type
1	I	inphase input	real
2	Q	quadrature input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	output	output data	int

Notes/Equations

1. This subnetwork is used to demodulate and decode the uplink baseband signal of coding scheme MCS5.
2. The schematic for this subnetwork is shown in the following figure. It consists of EDGE_BitSync, EDGE_Equalizer, EDGE_DeNormalBurst, EDGE_MCS5_UL_Decoder.

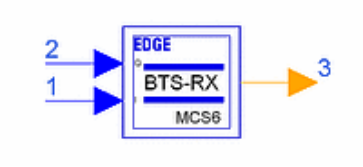


EDGE_BTS_MCS5_Receiver Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BTS_MCS6_Receiver



Description EDGE BTS MCS6 receiver
Library EDGE, BTS Test and Verification
Class SDFEDGE_BTS_MCS6_Receiver

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_Measured	time slot measured	0		int	[0, 7]
TSC	training sequence code	0		int	[0, 7]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†

† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$, Ji is the number of states on stage i, $1 \le i \le L$

Pin Inputs

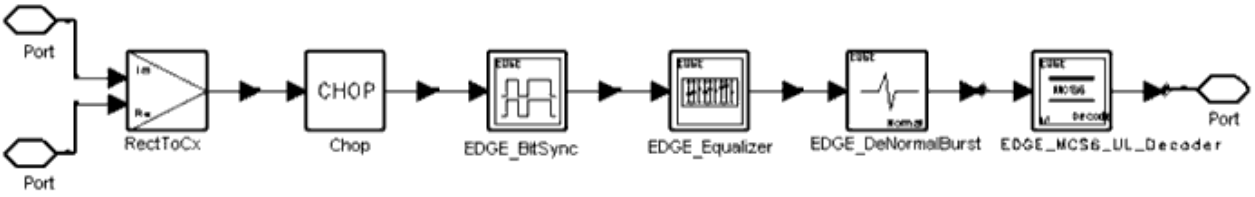
Pin	Name	Description	Signal Type
1	I	inphase input	real
2	Q	quadrature input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	output	output data	int

Notes/Equations

1. This subnetwork is used to demodulate and decode the uplink baseband signal of coding scheme MCS6.
2. The schematic for this subnetwork is shown in the following figure. It consists of EDGE_BitSync, EDGE_Equalizer, EDGE_DeNormalBurst, EDGE_MCS6_UL_Decoder.

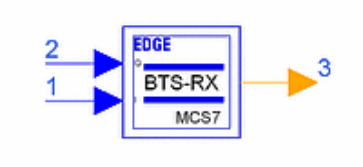


EDGE_BTS_MCS6_Receiver Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BTS_MCS7_Receiver



Description EDGE BTS MCS7 receiver
Library EDGE, BTS Test and Verification
Class SDFEDGE_BTS_MCS7_Receiver

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_Measured	time slot measured	0		int	[0, 7\]]
TSC	training sequence code	0		int	[0, 7\]]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5\]]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†

† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$, Ji is the number of states on stage i, $1 \le i \le L$

Pin Inputs

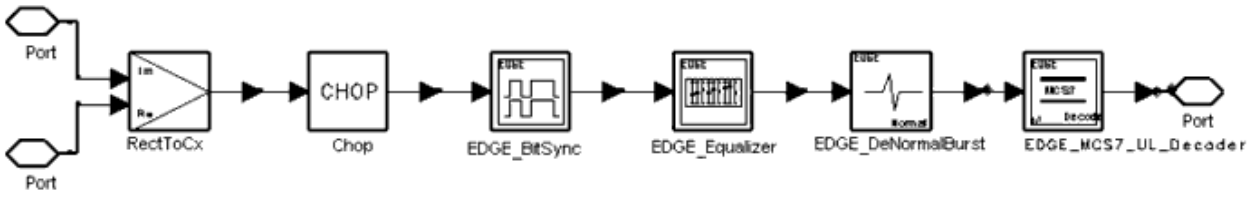
Pin	Name	Description	Signal Type
1	I	inphase input	real
2	Q	quadrature input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	output	output data	int

Notes/Equations

1. This subnetwork is used to demodulate and decode the uplink baseband signal of coding scheme MCS7.
2. The schematic for this subnetwork is shown in the following diagram. It consists of EDGE_BitSync, EDGE_Equalizer, EDGE_DeNormalBurst, EDGE_MCS7_UL_Decoder.

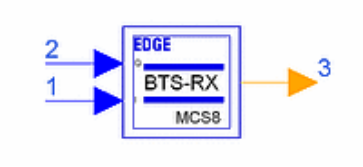


EDGE_BTS_MCS7_Receiver Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BTS_MCS8_Receiver



Description EDGE BTS MCS8 receiver
Library EDGE, BTS Test and Verification
Class SDFEDGE_BTS_MCS8_Receiver

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_Measured	time slot measured	0		int	[0, 7]
TSC	training sequence code	0		int	[0, 7]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†

† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$, Ji is the number of states on stage i, $1 \le i \le L$

Pin Inputs

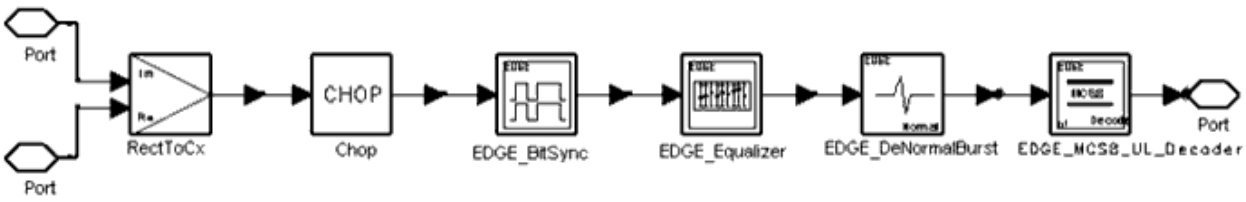
Pin	Name	Description	Signal Type
1	I	inphase input	real
2	Q	quadrature input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	output	output data	int

Notes/Equations

1. This subnetwork is used to demodulate and decode the uplink baseband signal of coding scheme MCS8.
2. The schematic for this subnetwork is shown in the following figure. It consists of EDGE_BitSync, EDGE_Equalizer, EDGE_DeNormalBurst, EDGE_MCS8_UL_Decoder.

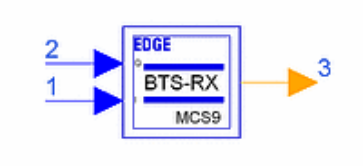


EDGE_BTS_MCS8_Receiver Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BTS_MCS9_Receiver



Description EDGE BTS MCS9 receiver
Library EDGE, BTS Test and Verification
Class SDFEDGE_BTS_MCS9_Receiver

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_Measured	time slot measured	0		int	[0, 7]
TSC	training sequence code	0		int	[0, 7]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†

† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$, Ji is the number of states on stage i, $1 \le i \le L$

Pin Inputs

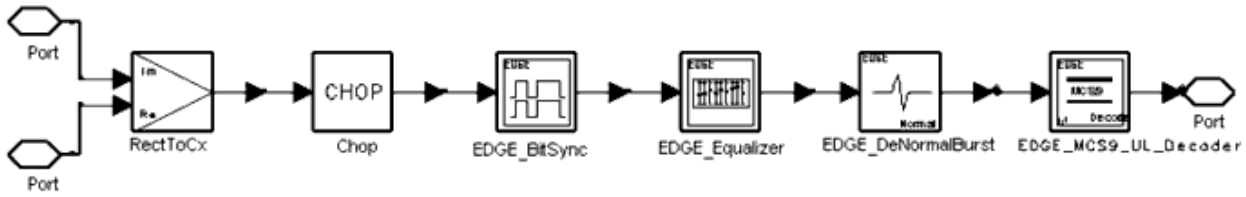
Pin	Name	Description	Signal Type
1	I	inphase input	real
2	Q	quadrature input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	output	output data	int

Notes/Equations

1. This subnetwork is used to demodulate and decode the uplink baseband signal of coding scheme MCS9.
2. The schematic for this subnetwork is shown in the following figure. It consists of EDGE_BitSync, EDGE_Equalizer, EDGE_DeNormalBurst, EDGE_MCS9_UL_Decoder.

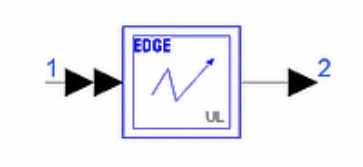


EDGE_BTS_MCS9_Receiver Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MultipathUp



Description Uplink multipath simulator for EDGE
Library EDGE, BTS Test and Verification
Class TSDFEDGE_MultipathUp

Name	Description	Default	Unit	Type	Range
Type	GSM type options: NoMultipath, RuralArea1, RuralArea2, HillyTerrain6Tap1, HillyTerrain6Tap2, HillyTerrain12Tap1, HillyTerrain12Tap2, UrbanArea6Tap1, UrbanArea6Tap2, UrbanArea12Tap1, UrbanArea12Tap2, EqualizationTest	NoMultipath		enum	
Pathloss	inclusion of large-scale pathloss: No, Yes	No		enum	
Seed	integer number to randomize the channel output	1234567		int	[1, ∞)
X	X-position coordinate of mobile antenna	100.0 meter	m	real	(-∞, ∞)
Y	Y-position coordinate of mobile antenna	0.0 meter	m	real	(-∞, ∞)
SpeedType	velocity unit option: km/hr, miles/hr	km/hr		enum	
Vx	X component of velocity vector	0.0		real	[0, ∞)
Vy	Y component of velocity vector	0.0		real	[0, ∞)

Pin Inputs

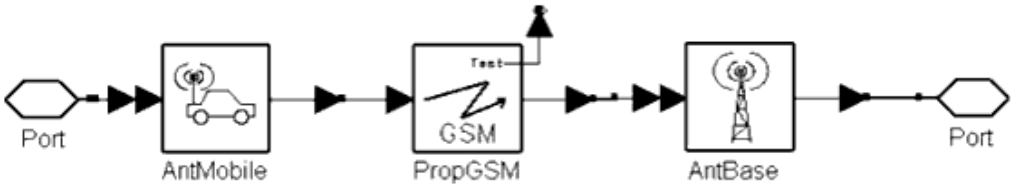
Pin	Name	Description	Signal Type
1	input	input RF signal	multiple timed

Pin Outputs

Pin	Name	Description	Signal Type
2	output	input RF signal	timed

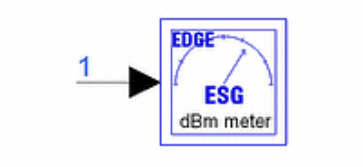
Notes/Equations

1. This subnetwork is used to simulate the uplink multipath channel for EDGE.
2. The schematic for this subnetwork is shown in the following figure. It consists of AntMobile, PropGSM, and AntBase that are used to simulate the mobile station antenna, the channel propagation condition, and the base station antenna, respectively.



EDGE_MultipathUp Schematic

EDGE_Pwr_Measure



Description Mean transmitted RF carrier power measurement
Library EDGE, BTS Test and Verification
Class TSDFEDGE_Pwr_Measure

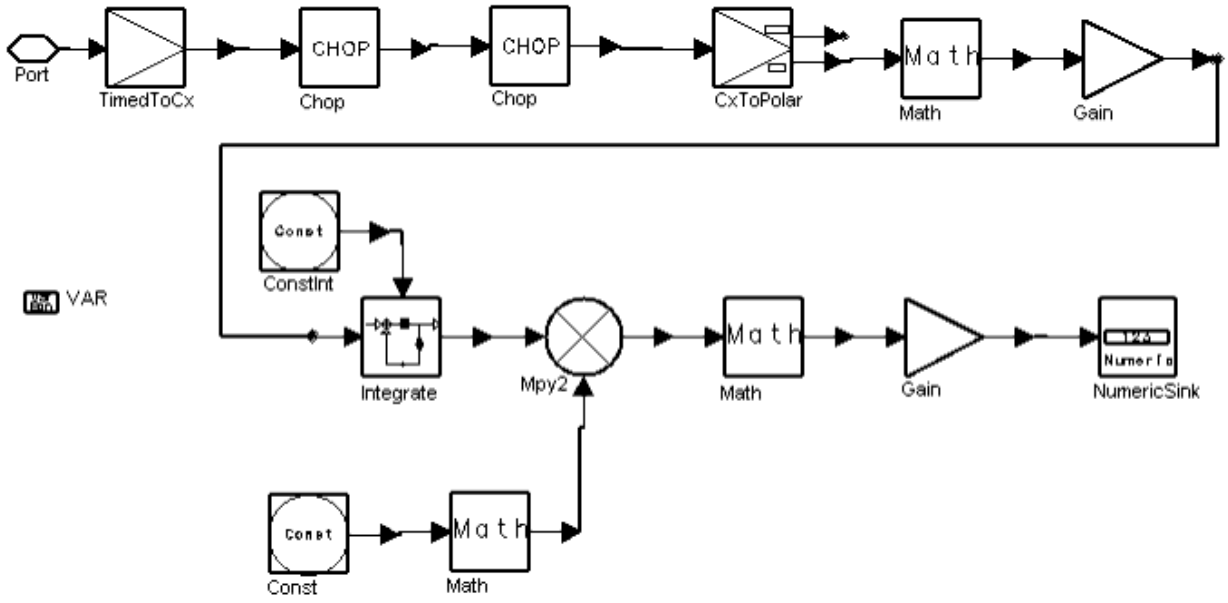
Name	Description	Default	Sym	Unit	Type	Range
BurstSpecVersion	EDGE specification for normal burst; if choose Basic, each burst has 156 symbols, otherwise complies with GSM 8.3.0 Release 1999: Basic, GSM_8_3_0_Release_1999	Basic			enum	
SampPerSym	number of samples per symbol	8	K		int	[1, ∞)
TS_Measured	time slot to be measured in each TDMA frame, 0 to 7	0			int	[0, 7]
TS_Num	number of time slots measured	100	M		int	[1, ∞)
SignalType	type of signal: Baseband signal, RF signal	Baseband signal			enum	
Rref	reference resistance	50.0		Ohm	real	[0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input signal	timed

Notes/Equations

1. This subnetwork is used to measure the mean transmitted RF carrier power. The schematic for this subnetwork is shown in the following figure.
   Each firing, one token is produced at output when M × 8 × 156 × K tokens are consumed at input.



EDGE_Pwr_Measure Schematic

2. If BurstSpecVersion is set to *Basic* , each burst in one TDMA frame of the input signal contain 156 symbols. 8 × 156 × K × M tokens are consumed each measurement.
   If BurstSpecVersion is set to *GSM_8_3_0_Release_1999* , the first and the fifth burst in one TDMA frame of the input signal contain 157 symbols, the other contain 156 symbols (as specified in GSM 05.02, version 8.3.0, Release 1999).
   (2 × 157+6 × 156) × K × M tokens are consumed each measurement.
3. The signal power measurement equation is

$$P_s = 10\log\left(\frac{1000}{L \times R_{ref}} \sum_{n=0}^{N-1} |S_n|^2\right)$$

   where

   N = (156-G) × M × K is the total number of samples measured

   G is the number of guard symbols in a burst

   Sn is the input signal sample

   L =1 if the input signal is baseband ; *L* =2 if the input signal is RF

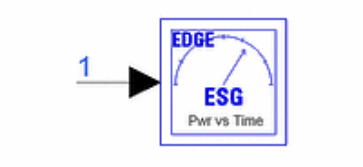
The unit of *P* s is dBm.

Guard symbols are ignored in signal power measurement.

References

1. 6.3 of GSM 11.21, version 7.2.0 Release 1998
2. ETSI Tdoc SMG2 530/00, CR 11.21-A122 EDGE TX-test cases and uncertainties, April 04-07, 2000.

EDGE_Pwr_vs_Time



Description Power vs time measurement for EDGE
Library EDGE, BTS Test and Verification
Class TSDFEDGE_Pwr_vs_Time

Parameters

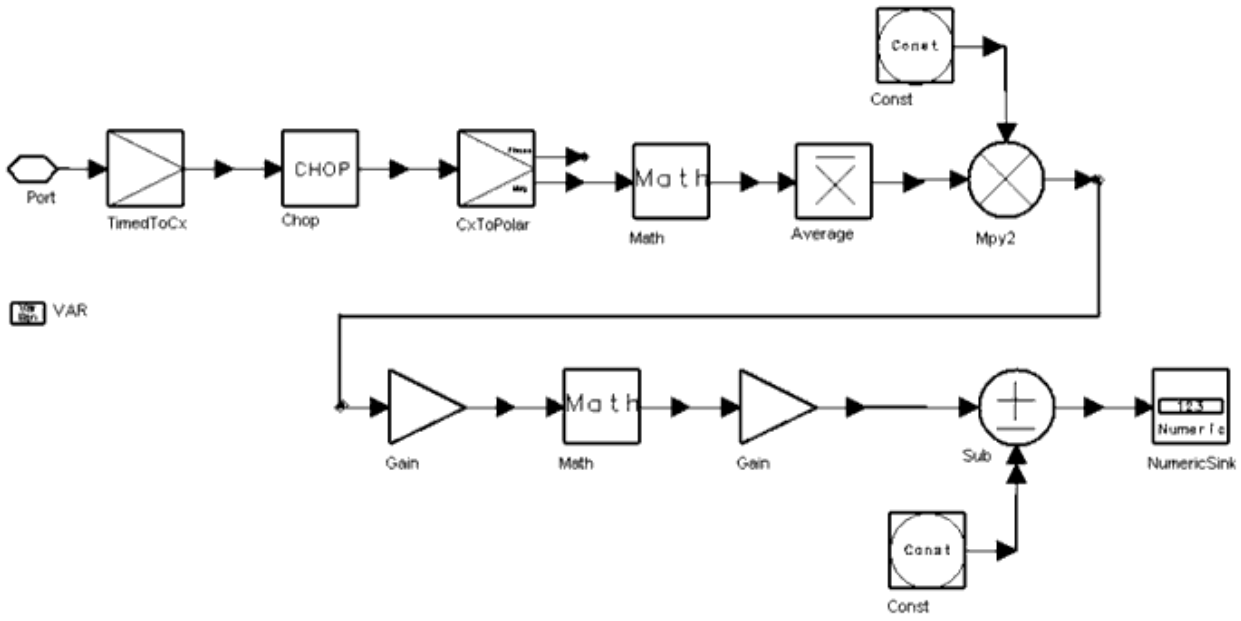
Name	Description	Default	Sym	Unit	Type	Range
BurstSpecVersion	EDGE specification for normal burst; if choose Basic, each burst has 156 symbols, otherwise complys with GSM 8.3.0 Release 1999: Basic, GSM_8_3_0_Release_1999	Basic			enum	
SampPerSym	number of samples per symbol	8	K		int	[1, ∞)
TS_Measured	time slot to be measured in each TDMA frame,0 to 7.	0			int	[0, 7]
TS_Num	number of time slots measured	100	M		int	[1, ∞)
SignalType	type of signal: Baseband signal, RF signal	Baseband signal			enum	
Rref	reference resistance	50.0 Ohm		Ohm	real	[0, ∞)
Mean_Tx_Pwr	mean transmitted power, in dBm	12			real	

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input RF data to be measured	timed

Notes/Equations

1. This subnetwork is used to measure the transmitted RF carrier power versus time of the input signal. The schematic is shown in the following figure.
2. If BurstSpecVersion is set to *Basic* , each burst in one TDMA frame of the input signal contains 156 symbols. 8 × 156 × K × M tokens are consumed each measurement. If BurstSpecVersion is set to *GSM_8_3_0_Release_1999* , the first and the fifth bursts in one TDMA frame of the input signal each contain 157 symbols, the others contain 156 symbols, as specified in GSM 05.02, version 8.3.0, Release 1999. (2 × 157 + 6 × 156) × K × M tokens are consumed each measurement.
3. Because the mask for power versus time (as specified in Reference 1 occupies the duration of 162 symbols, 162 × K tokens are generated once a measurement.
4. Set the Mean_Tx_Power parameter to the input signal mean power for normalization purposes.



EDGE_Pwr_vs_Time

References

1. 13.17.3 of ETSI Tdoc SMG7 022/00, version 420, CR 11.10 Introduction of EGPRS Transmitter Tests for Frequency Error, Power, ORFS and Intermodulation Attenuation, March 22-24, 2000.

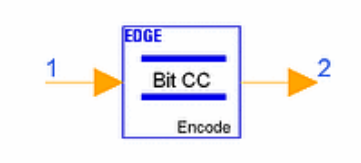
2. GSM 05.02, version 8.3.0, Release 1999.

Channel Coding Components for EDGE Design Library

- *EDGE BitCC* (edge)
- *EDGE BitDeSwapping* (edge)
- *EDGE BitSwapping* (edge)
- *EDGE BurstDeMapping* (edge)
- *EDGE BurstMapping* (edge)
- *EDGE CC WithTail* (edge)
- *EDGE Combiner* (edge)
- *EDGE CycDecoder* (edge)
- *EDGE CycEncoder* (edge)
- *EDGE DCC WithTail* (edge)
- *EDGE DeInterleaver* (edge)
- *EDGE DePuncture* (edge)
- *EDGE ExtraSFAddRmv* (edge)
- *EDGE HeaderDeIntrlv* (edge)
- *EDGE HeaderDePunc* (edge)
- *EDGE HeaderIntrlv* (edge)
- *EDGE HeaderPunc* (edge)
- *EDGE Interleaver* (edge)
- *EDGE MCS1 DL Decoder* (edge)
- *EDGE MCS1 DL Encoder* (edge)
- *EDGE MCS1 UL Decoder* (edge)
- *EDGE MCS1 UL Encoder* (edge)
- *EDGE MCS2 DL Decoder* (edge)
- *EDGE MCS2 DL Encoder* (edge)
- *EDGE MCS2 UL Decoder* (edge)
- *EDGE MCS2 UL Encoder* (edge)
- *EDGE MCS3 DL Decoder* (edge)
- *EDGE MCS3 DL Encoder* (edge)
- *EDGE MCS3 UL Decoder* (edge)
- *EDGE MCS3 UL Encoder* (edge)
- *EDGE MCS4 DL Decoder* (edge)
- *EDGE MCS4 DL Encoder* (edge)
- *EDGE MCS4 UL Decoder* (edge)
- *EDGE MCS4 UL Encoder* (edge)
- *EDGE MCS5 DL Decoder* (edge)
- *EDGE MCS5 DL Encoder* (edge)
- *EDGE MCS5 UL Decoder* (edge)
- *EDGE MCS5 UL Encoder* (edge)
- *EDGE MCS6 DL Decoder* (edge)
- *EDGE MCS6 DL Encoder* (edge)
- *EDGE MCS6 UL Decoder* (edge)
- *EDGE MCS6 UL Encoder* (edge)
- *EDGE MCS7 DL Decoder* (edge)
- *EDGE MCS7 DL Encoder* (edge)
- *EDGE MCS7 UL Decoder* (edge)
- *EDGE MCS7 UL Encoder* (edge)
- *EDGE MCS8 DL Decoder* (edge)
- *EDGE MCS8 DL Encoder* (edge)
- *EDGE MCS8 UL Decoder* (edge)
- *EDGE MCS8 UL Encoder* (edge)

- *EDGE MCS9 DL Decoder* (edge)
- *EDGE MCS9 DL Encoder* (edge)
- *EDGE MCS9 UL Decoder* (edge)
- *EDGE MCS9 UL Encoder* (edge)
- *EDGE Puncture* (edge)
- *EDGE RSDecoder* (edge)
- *EDGE RSEncoder* (edge)
- *EDGE Splitter* (edge)
- *EDGE TailBits* (edge)
- *EDGE USFPostDecoder* (edge)
- *EDGE USFPreEncoder* (edge)
- *EDGE ViterbiBitDCC* (edge)

EDGE_BitCC



Description Convolutional encoder bit by bit.
Library EDGE, Channel Coding
Class SDFEDGE_BitCC
Derived From EDGE_CnvlCoder

Parameters

Name	Description	Default	Sym	Type	Range
CodeRate	convolutional code rate.	2	N	int	†
ConstraintLength	convolutional code constraint length.	9	K	int	(1, 9]
Polynomials	convolutional code polynomials, in terms of octal number	0753 0561		int array	††

† CodeRate ≥ 1. Reciprocals are used to represent fractional code rates: 1 = code rate 1; 2 = code rate 1/2; 3 = code rate 1/3.† † Octal numbers are used to indicate generator polynomials; one digit in an octal number corresponds to 3 digits in a binary number; the bit number of each polynomial can be evenly divided by 3. If the constraint length (assumed to be K) cannot be evenly divided by 3, only higher K generator bits are used; other (lower) bits are all 0s. The MSB represents the term without delay in the polynomial; delay increases left to right. For example, the generator g0 is $1+D^3+D^4+D^5+D^6$, which has a constraint length of 7; the polynomials are written as 100111100 (that is, 0474).

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be convolutionally encoded.	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	convolutionally encoded symbols	int

Notes/Equations

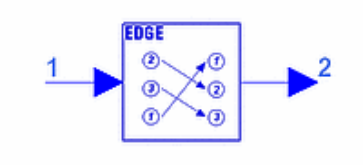
This model is used to convolutionally encode the input bit.

CodeRate output tokens are produced when one input token is consumed.

References

1. S. Lin and D. J. Costello, Jr., *Error Control Coding Fundamentals and Applications* , Prentice Hall, Englewood Cliffs NJ, 1983.

EDGE_BitDeSwapping



Description Bit de-swapping in normal burst
Library EDGE, Channel Coding
Class SDFEDGE_BitDeSwapping

Parameters

Name	Description	Default	Type	Range
Pos1	bit positions to be swapped with those defined in Pos2	142 144 145 147 148 150 151 176 179 182 185 188 191 194	int array	†
Pos2	bit positions to be swapped with those defined in Pos1	155 158 161 164 167 170 173 195 196 198 199 201 202 204	int array	†
† The size of Pos1 must be equal to the size of Pos2; the value of each element in Pos1 and Pos2 must be in the range [0,347]. Default values are set according to [1]				

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bit-swapped burst	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	bit de-swapped burst	real

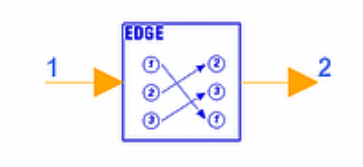
Notes/Equations

1. The model is used to perform bit de-swapping to each input information block of a normal burst.
   Each firing, 348 tokens are produced when 348 tokens are consumed.
2. In channel coding schemes MCS_5 to MCS_9, bit swapping must be performed to each 348-bit data block that is mapped to a burst. Pos1 and Pos2 define the swapping scheme and can be set by the designer.

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BitSwapping



Description Bit swapping in normal burst
Library EDGE, Channel Coding
Class SDFEDGE_BitSwapping

Parameters

Name	Description	Default	Type	Range
Pos1	bit positions to be swapped with those defined in Pos2	142 144 145 147 148 150 151 176 179 182 185 188 191 194	int array	†
Pos2	bit positions to be swapped with those defined in Pos1	155 158 161 164 167 170 173 195 196 198 199 201 202 204	int array	†
† The size of Pos1 must be equal to the size of Pos2; the value of each element in Pos1 and Pos2 must be in the range of [0, 347]. Default values are set according to [1\]				

Pin Inputs

Pin	Name	Description	Signal Type
1	input	burst to be bit-swapped	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	burst after bit-swapping	int

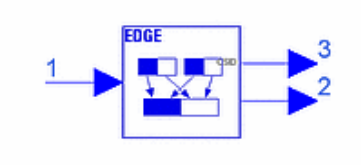
Notes/Equations

1. The model is used to perform bit swapping to each input information block of a normal burst.
   Each firing, 348 tokens are produced when 348 tokens are consumed.
2. In channel coding schemes MCS_5 to MCS_9, bit swapping must be performed to each 348-bit data block that is mapped to a burst. Pos1 and Pos2 define the swapping scheme and can be set by the designer.

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BurstDeMapping



Description Normal burst demapping
Library EDGE, Channel Coding
Class SDFEDGE_BurstDeMapping

Parameters

Name	Description	Default	Type
CodingScheme	type of coding scheme: CS_1, CS_2, CS_3, CS_4, MCS_1, MCS_2, MCS_3, MCS_4, MCS_5, MCS_6, MCS_7, MCS_8, MCS_9	CS_1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	information bits including CSID	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	information bits	real
3	CSID	channel coding scheme identification bits	real

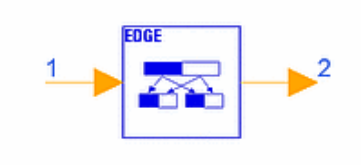
Notes/Equations

1. This model is used to remove coding scheme identification bits from each burst and combine each four bursts into one data block for decoding.
   Each firing, BurstLen−2 tokens are produced at output and two tokens are produced at CSID when BurstLen tokens are consumed, where BurstLen is the number of encrypted bits in one burst. For coding schemes used with GMSK modulation (CS1 to CS4 and MCS_1 to MCS_4), BurstLen is 116; for coding schemes with 8PSK modulation (MCS_5 to MCS_9), BurstLen is 348.
2. Before de-interleaving, de-puncturing and channel decoding, two coding scheme identification bits must be removed from each burst. Data bits of four bursts must then be combined into a decoding block. Before decoding, different parts of the block (USF for downlink, header and data) will be split by EDGE_Splitter. The eight coding scheme identification bits of four bursts are used to detect the channel coding scheme.

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BurstMapping



Description Normal burst mapping
Library EDGE, Channel Coding
Class SDFEDGE_BurstMapping

Parameters

Name	Description	Default	Type
CodingScheme	type of coding scheme: CS_1, CS_2, CS_3, CS_4, MCS_1, MCS_2, MCS_3, MCS_4, MCS_5, MCS_6, MCS_7, MCS_8, MCS_9	CS_1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	channel coded bits	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	bits mapped into 4 bursts	int

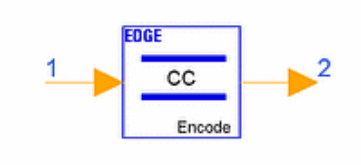
Notes/Equations

1. The model is used to map the channel encoded block into four bursts.
   Each firing, BurstLen tokens are produced when BurstLen-2 tokens are consumed, where BurstLen is the number of encrypted bits in one burst. For coding schemes used with GMSK modulation (CS_1 to CS_4 and MCS_1 to MCS_4), BurstLen is 116; for coding schemes with 8PSK modulation (MCS_5 to MCS_9), BurstLen is 348.
2. After channel coding, puncturing and interleaving, different parts of bits (USF in downlink, header and data) are combined by EDGE_Combiner. This model divides the combined data block into four sub-blocks and maps each sub-block to one burst. In burst mapping, two bits that identify the coding scheme are inserted into each sub-block.

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_CC_WithTail



Description Convolutional encoder with tail
Library EDGE, Channel Coding
Class SDFEDGE_CC_WithTail
Derived From EDGE_CnvlCoder

Parameters

Name	Description	Default	Sym	Type	Range
CodeRate	convolutional code rate.	2	N	int	†
ConstraintLength	convolutional code constraint length.	9	K	int	(1, 9]
Polynomials	convolutional code polynomials, in terms of octal number	0753 0561		int array	††
InputFrameLength	length of input frame	96		int	[K, ∞)

† CodeRate ≥ 1. Reciprocals are used to represent fractional code rates: 1 = code rate 1; 2 = code rate 1/2; 3 = code rate 1/3.† † Octal numbers are used to indicate generator polynomials; one digit in an octal number corresponds to 3 digits in a binary number; the bit number of each polynomial can be evenly divided by 3. If the constraint length (assumed to be K) cannot be evenly divided by 3, only higher K generator bits are used; other (lower) bits are all 0s. The MSB represents the term without delay in the polynomial; delay increases left to right. For example, the generator g0 is $1+D^3+D^4+D^5+D^6$, which has a constraint length of 7; the polynomials are written as 100111100 (that is, 0474).

Pin Inputs

Pin	Name	Description	Signal Type
1	input	data to be convolutionally encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	convolutionally encoded symbols	int

Notes/Equations

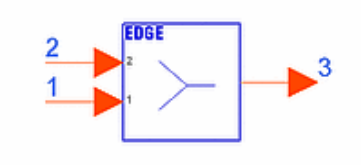
This model is used to convolutionally encode the input tailed frame.

InputFrameLength × CodeRate output tokens are produced when InputFrameLength input tokens are consumed.

References

1. S. Lin, D. J. Costello, Jr., Error Control Coding Fundamentals and Applications, Prentice Hall, Englewood Cliffs NJ, 1983.

EDGE_Combiner



Description Bits combiner for channel coding
Library EDGE, Channel Coding
Class SDFEDGE_Combiner

Parameters

Name	Description	Default	Sym	Type	Range
Length1	block length of input1	6	N1	int	(0, ∞)
Length2	block length of input2	284	N2	int	(0, ∞)
CombineMode	combination mode: input1 to be first part, input2 to be first part, input1 to be middle part, input2 to be middle part	input1 to be first part		enum	

Pin Inputs

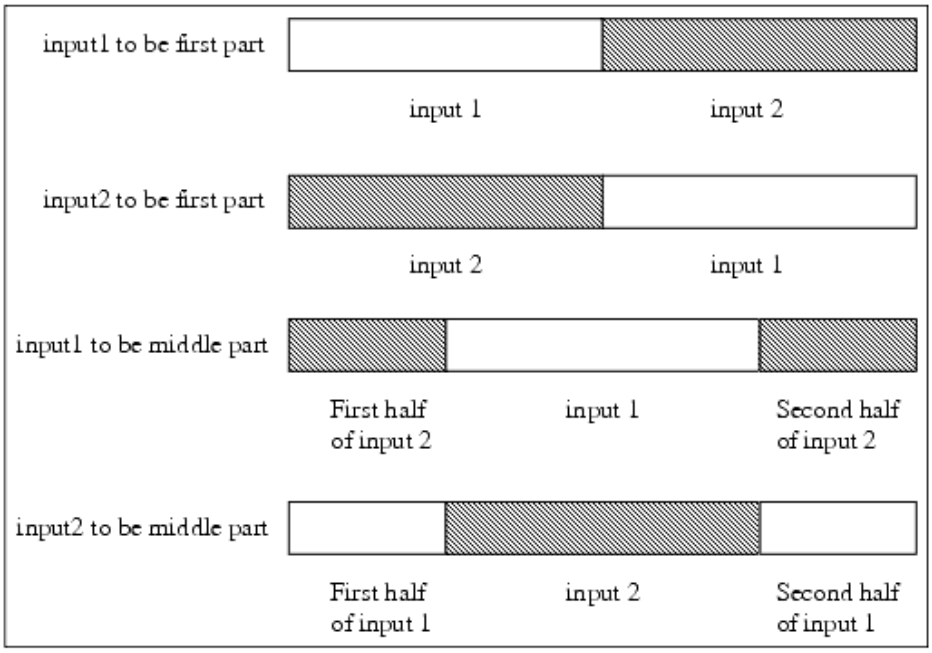
Pin	Name	Description	Signal Type
1	input1	input block 1	anytype
2	input2	input block 2	anytype

Pin Outputs

Pin	Name	Description	Signal Type
3	output	combination of input1 and input2	anytype

Notes/Equations

1. The model is used to combine two input data blocks into one output data block. Each firing, N1+N2 output tokens are produced when N1 tokens are consumed at input1 and N2 tokens are consumed at input2.
2. In EDGE channel coding, different parts of data bits (USF in downlink, header and data) must be combined in a certain way. This model is used combine two input data blocks; to combine three data blocks, two combiners can be used in a cascade.
   The combining pattern is determined by the CombineMode setting and illustrated in the following figure.
   - When CombineMode = input1 to be first part (or input2 to be first part), data of input1 (or input2) is output first.
   - When CombineMode = input1 to be middle part (or input2 to be middle part), first half of input2 (or input1) is output first, then the other input and the second half of input2 (or input1) is output.
     When the length of the input block that will be split to the front and rear parts of the output is odd, the number of bits in the first half will be one less than that of the second half.

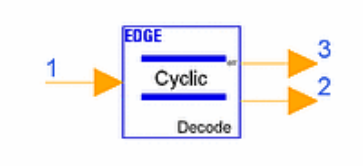


CombineMode Combining Pattern

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_CycDecoder



Description Systematic cyclic codes decoder
Library EDGE, Channel Coding
Class SDFEDGE_CycDecoder

Parameters

Name	Description	Default	Sym	Type	Range
ShortenFlag	flag indicating a shortened code: Not Shortened Code, Shortened Code	Shortened Code		enum	†
CorrectFlag	flag indicating to correct errors: Detection Only, Detection and Correction	Detection Only		enum	
CodeLength	length of code word	53	n	int	(0, ∞) ††
InfoLength	length of information part in code word	50	k	int	(0, CodeLength) †††
GenType	type of generator polynomial selector: Using Enum Type selector GenEnum, Using Array Type selector GenArray	Using Enum Type selector GenEnum		enum	
GenEnum	generator polynomial, valid when GenType = 0: g 13, g 157, g 2565	g 13		enum	
GenArray	generator polynomial, in octal, MSB first, valid when GenType = 1	1 3		int array	[0, 7] ‡
CutOffBits	number of bits cut off in shortened cyclic code	0	ss	int	(0, ∞)

† ShortenFlag is not used when CorrectFlag=Detection Only;CutOffBits is only used when CorrectFlag=Detection and Correction and ShortenFlag=Shortened Code†† ($D^{CodeLength} + 1$) should be divisible by g(D) when ShortenFlag = Not Shortened Code and CorrectFlag = Detection and Correction, or ($D^{CodeLength+CutOffBits} + 1$) should be divisible by g(D) when ShortenFlag = Shortened Code and CorrectFlag = Detection and Correction, where g(D) is the generator polynomial specified by GenEnum or GenArray.††† CodeLength - InfoLength = order of g(D).‡ The last element in an array must be an odd number.

Pin Inputs

Pin	Name	Description	Signal Type
1	input	received code word	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	decoded information block	int
3	errMsg	message indicating an error that cannot be corrected	int

Notes/Equations

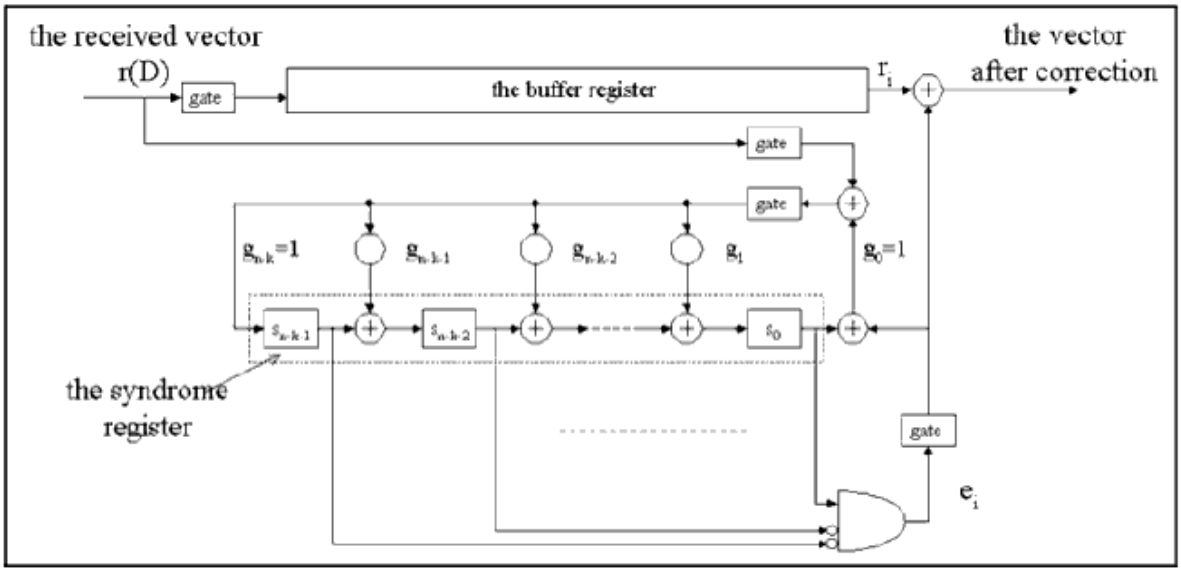
1. This model is used to decode cyclically encoded data. InfoLength output tokens and one errMsg token are produced for each CodeLength input token consumed.
2. The decoder used here is the Meggit decoder [1, 2], shown in the following figure, where

   $$r(D) = r_0 D^{n-1} + r_1 D^{n-2} + \ldots + r_{n-2} D + r_{n-1}$$

   is the polynomial of the received code word, g_i, i = 0, 1, ... , n−k, are the coefficients of the generator polynomial g(D)

   $$g(D) = g_0 D^{n-k} + g_1 D^{n-k-1} + \ldots + g_{n-k-1} D + g_{n-k}$$

   The decoder is designed to correct, at most, one error in a code word.

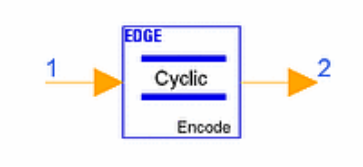


Cyclic Codes Decoder with Received Polynomial r(D) Shifted into the Syndrome Register from the Right

References

1. J. E. Meggit, "Error Correcting Codes and Their Implementation," *IRE Trans. Inform. Theory* , IT-7, pp. 232-244, Oct. 1961.
2. S. Lin and D. J. Costello, Jr., *Error Control Coding Fundamentals and Applications* , Prentice Hall, Englewood Cliffs NJ, 1983.

EDGE_CycEncoder



Description Systematic cyclic codes encoder
Library EDGE, Channel Coding
Class SDFEDGE_CycEncoder

Parameters

Name	Description	Default	Sym	Type	Range
CodeLength	length of code word	53	n	int	(0, ∞) †
InfoLength	length of information part in code word	50	k	int	(0, CodeLength) ††
GenType	type of generator polynomial selector: Using Enum Type selector GenEnum, Using Array Type selector GenArray	Using Enum Type selector GenEnum		enum	
GenEnum	generator polynomial, valid when GenType = 0: g 13, g 157, g 2565, g 45045, g 123, g 20000440400011	g 13		enum	
GenArray	generator polynomial, in octal, MSB first, valid when GenType = 1	1 3		int array	[0, 7] †††

† ($D^{CodeLength} + 1$) should be divisible by g(D), where g(D) is the generator polynomial specified by GenEnum or GenArray.†† CodeLength - InfoLength = order of g(D).††† The last element in an array must be an odd number.

Pin Inputs

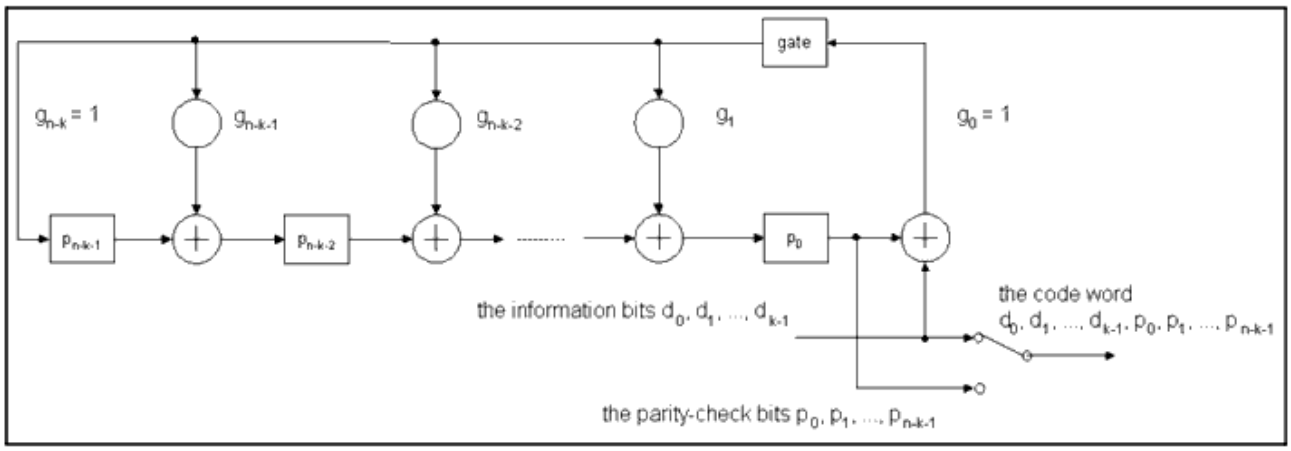
Pin	Name	Description	Signal Type
1	input	information block to be encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	code word in systematic form	int

Notes/Equations

1. This model is used to encode input data into cyclic codes. CodeLength output tokens are produced for each InfoLength token consumed.
2. The encoding circuit of the systematic cyclic codes is shown in the following diagram. It is a dividing circuit. The gate opens while the information bits are shifted into the circuit. After all data are read, the n − k bits in the registers become the parity-check bits. And the gate closes, the switch changes to the lower position to shift out the parity bits.



Systematic Cyclic Codes Encoding Circuit

The cyclic codes used in GSM channels are:

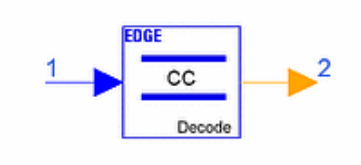
- TCH/FS: n = 53, k = 50, $g(D) = D^3 + D + 1$;
- RACH: n = 14, k = 8, $g(D) = D^6 + D^5 + D^3 + D^2 + D + 1$;
- SCH: n = 35, k = 25, $g(D) = D^{10} + D^8 + D^6 + D^5 + D^4 + D^2 + 1$;
- SACCH, BCCH, PCH, AGCH, CBCH, SDCCH, FACCH: n=224, k=184, $g(D) = (D^{17} + D^3 + 1)(D^{23} + 1) = D^{40} + D^{26} + D^{23} + D^{17} + D^3 + 1$ (Fire code).

To agree with GSM05.03, that is, when divided by g(D), the code word yields a remainder equal to $1 + D + D^2 + \ldots + D^{(\text{CodeLength-InfoLength-1})}$. The parity-check bits are reversed before they are added to the end of information bits.

References

1. S. Lin and D. J. Costello, Jr., *Error Control Coding Fundamentals and Applications* , Prentice Hall, Englewood Cliffs NJ, 1983.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.03, *Channel Coding* , version 5.1.0, May 1996.

EDGE_DCC_WithTail



Description Viterbi decoder for convolutional code with tail
Library EDGE, Channel Coding
Class SDFEDGE_DCC_WithTail
Derived From EDGE_ViterbiDecoder

Parameters

Name	Description	Default	Sym	Type	Range
CodeRate	convolutional code rate.	2	N	int	†
ConstraintLength	convolutional code constraint length.	9	K	int	(1, 9]
Polynomials	convolutional code polynomials, in terms of octal number	0753 0561		int array	††
InputFrameLength	length of input frame.	288		int	[N, ∞)

† CodeRate ≥ 1. Reciprocals are used to represent fractional code rates: 1 = code rate 1; 2 = code rate 1/2; 3 = code rate 1/3.†† Octal numbers are used to indicate generator polynomials; one digit in an octal number corresponds to 3 digits in a binary number; the bit number of each polynomial can be evenly divided by 3. If the constraint length (assumed to be K) cannot be evenly divided by 3, only higher K generator bits are used; other (lower) bits are all 0s. The MSB represents the term without delay in the polynomial; delay increases left to right. For example, the generator g0 is $1+D^3+D^4+D^5+D^6$ which has a constraint length of 7; the polynomials are written as 100111100 (that is, 0474).

Pin Inputs

Pin	Name	Description	Signal Type
1	input	symbols to be decoded.	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	decoded bits.	int

Notes/Equations

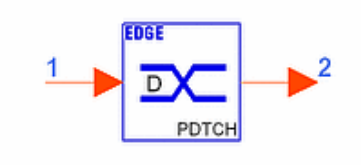
This model is used to Viterbi-decode convolutional code with tail.

InputFrameLength/CodeRate output tokens are produced when InputFrameLength input tokens are consumed.

References

1. S. Lin and D. J. Costello, Jr., *Error Control Coding Fundamentals and Applications* , Prentice Hall, Englewood Cliffs NJ, 1983.
2. R. Steele, Mobile Radio Communic *ations* , London: Pentech Press, 1992.

EDGE_DeInterleaver



Description De-interleaving for packet data traffic channels
Library EDGE, Channel Coding
Class SDFEDGE_DeInterleaver
Derived From EDGE_Interleaver

Parameters

Name	Description	Default	Type
CodingScheme	type of coding scheme: CS1-4&MCS1-4, MCS5-6, MCS7, MCS8-9	CS1-4&MCS1-4	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	convolutionally encoded and punctured symbols.	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	output	interleaved symbols.	anytype

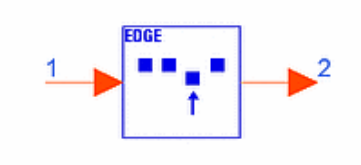
Notes/Equations

1. This model is used to de-interleave packet data traffic channels of EDGE; it is the inverse of the EDGE_Interleaver process.
   Input and output data lengths depend on the CodingScheme parameter:
   - for CS1-4&MCS1-4, 456 symbols are consumed at input and produced at output
   - for MCS5-6, 1248 symbols are consumed at input and produced at output
   - for MCS7 and MCS8-9, 1224 symbols are consumed at input and produced at output.
2. For naming conventions and interleaving rules of MCS and CS coding schemes, refer to EDGE_Interleaver.

References

1. ETSI SMG2 EDGE Tdoc 999/99, CR 05.03-A025 EGPRS Channel Coding, Bordeaux, France, September 20-24, 1999.
2. ETSI SMG2 EDGE Tdoc 278/99, EGPRS Channel Coding, Paris, France, 24-27 August 1999.

EDGE_DePuncture



Description Data de-puncturing
Library EDGE, Channel Coding
Class SDFEDGE_DePuncture

Parameters

Name	Description	Default	Type	Range
CodingScheme	type of coding scheme: CS_2, CS_3, MCS_1, MCS_2, MCS_3, MCS_4, MCS_5, MCS_6, MCS_7, MCS_8, MCS_9	MCS_1	enum	
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum	†
† P1 is the only puncturing scheme for CS2 and CS3 coding schemes; P3 is the only puncturing scheme for MCS3, 4, 7, 8, and 9.				

Pin Inputs

Pin	Name	Description	Signal Type
1	input	punctured convolutionally encoded symbols	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	output	depunctured convolutionally encoded symbols	anytype

Notes/Equations

This model depunctures the punctured convolutionally encoded symbols by inserting 0s at the positions where data has been punctured.

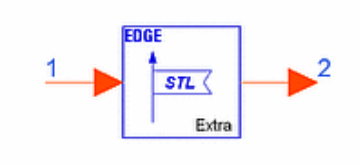
There are no puncturing schemes in CS1 and CS4. Each firing:

- 588 bits are produced at output while 456 bits are consumed at input, when M = CS2;
- 676 bits are produced at output while 456 bits are consumed at input, when M = CS3;
- 588 bits are produced at output while 372 bits are consumed at input, when M = MCS_1;
- 732 bits are produced at output while 372 bits are consumed at input, when M = MCS_2;
- 948 bits are produced at output while 372 bits are consumed at input, when M = MCS_3;
- 1116 bits are produced at output while 372 bits are consumed at input, when M = MCS_4;
- 1404 bits are produced at output while 1248 bits are consumed at input, when M = MCS_5;
- 1836 bits are produced at output while 1248 bits are consumed at input, when M = MCS_6;
- 1404 bits are produced at output while 612 bits are consumed at input, when M = MCS_7;
- 1692 bits are produced at output while 612 bits are consumed at input, when M = MCS_8;
- 1836 bits are produced at output while 612 bits are consumed at input, when M = MCS_9;

References

1. ETSI TDOC SMG2 EDGE 999/99, CR 05.03-A025 EGPRS Channel Coding, Bordeaux, France, September 20-24, 1999.
2. ETSI TDOC SMG2 EDGE 278/99, EGPRS Channel Coding, Paris, France, 24-27 August 1999.

EDGE_ExtraSFAddRmv



Description Add or remove extra stealing flags for MCS1 to MCS4
Library EDGE, Channel Coding
Class SDFEDGE_ExtraSFAddRmv

Parameters

Name	Description	Default	Type
Action	add or remove extra stealing flags: add extra SF, remove extra SF	add extra SF	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input data block	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output data block	anytype

Notes/Equations

1. This model is used for adding or removing the four extra stealing flags into or from the input data block.
   Each firing, OutputLen tokens are produced when InputLen tokens are consumed. The values of InputLen and OutputLen depend on the setting of Action as listed in the following table.

Action	InputLen	OutputLen
add extra SF	452	456
remove extra SF	456	452

2. In MCS1 to MCS4, four extra stealing flags must be added into the data block that is to be interleaved. The adding pattern is:

   $c'(n,25) = q(8)$

   $c'(n,82) = q(9)$

   $c'(n,139) = q(10)$

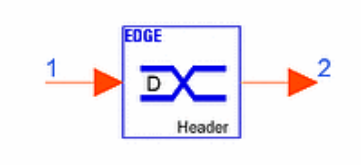
   $c'(n,424) = q(11)$

   where q(8), q(9), ... , q(11) = 0, 0, 0, 0 are the four extra stealing flags. In channel decoding, these extra stealing flags must be removed from the data block to be de-interleaved.

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_HeaderDeIntrlv



Description Header de-interleaver
Library EDGE, Channel Coding
Class SDFEDGE_HeaderDeIntrlv
Derived From EDGE_HeaderIntrlv

Parameters

Name	Description	Default	Type
CodingScheme	type of coding scheme: MCS5-6, MCS7-9	MCS5-6	enum
LinkType	type of link: DownLink, UpLink	DownLink	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input data block	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output data block	anytype

Notes/Equations

1. This model is used for de-interleaving header bits in modulation and coding schemes MCS5 to MCS9.
   Each firing, N output tokens are produced when N input tokens are consumed; refer to the following table.

   N Values

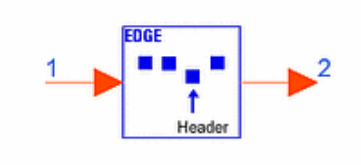
CodingScheme	LinkType	N
MCS5-6	DownLink	100
	UpLink	136
MCS7-9	DownLink	124
	UpLink	160

2. Header Interleaving Rules
   MCS5-6 Downlink
   The 100 coded bits of the header, {hc(0), hc(1), ... , hc(99)}, are interleaved according to:
   hi(j) = hc(k) for k = 0, 1, ... , 99
   j = 25(k mod 4) + ((17k) mod 25)
   MCS5-6 Uplink
   The 136 coded bits of the header, {hc(0), hc(1), ... , hc(135)}, are interleaved according to:
   hi(j) = hc(k) for k = 0, 1, ... , 135
   j = 34(k mod 4) + 2((11k) mod 17) + [(k mod 8)/4]
   MCS7-9 Downlink
   The 124 coded bits of the header, {hc(0), hc(1), ... , hc(123)}, are interleaved according to:
   hi(j) = hc(k) for k = 0, 1, ... , 123
   j = 31(k mod 4) + ((17k) mod 31)
   MCS7-9 Uplink
   The 160 coded bits of the header, {hc(0), hc(1), ... , hc(159)}, are interleaved according to:
   hi(j) = hc(k) for k = 0, 1, ... , 159
   j = 40(k mod 4) + 2((13(k div 8)) mod 20) + ((k mod 8) div 4)

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_HeaderDePunc



Description Header de-puncture
Library EDGE, Channel Coding
Class SDFEDGE_HeaderDePunc
Derived From EDGE_HeaderPunc

Parameters

Name	Description	Default	Type
CodingScheme	type of coding scheme: MCS1-4, MCS5-6, MCS7-9	MCS1-4	enum
LinkType	type of link: DownLink, UpLink	DownLink	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input data block	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output data block	anytype

Notes/Equations

1. This model is used for de-puncturing header bits in modulation and coding schemes MCS1 to MCS9.
   Each firing, OutputLen output tokens are produced when InputLen input tokens are consumed; refer to the following table.

   InputLen and OutputLen Values

CodingScheme	LinkType	InputLen	OutputLen
MCS1-4	DownLink	68	108
	UpLink	80	117
MCS5-6	DownLink	100	99
	UpLink	136	135
MCS7-9	DownLink	124	135
	UpLink	160	162

2. Header Puncturing Rules
   MCS1-4 Downlink
   The code is punctured in such a way that these coded bits are not transmitted:
   {C(2+3j) for j = 0, 1, ... , 35}
   as well as
   {C(k) for k = 34, 58, 82, 106}
   The result is a block of 68 coded bits, {hc(0), hc(1), ... , hc(67)}.
   MCS1-4 Uplink
   The code is punctured in such a way that these coded bits are not transmitted:
   {C(5+12j), C(8+12j), C(11+12j), for j = 0, 1, ... , 8}
   as well as
   {C(k) for k = 26, 38, 50, 62, 74, 86, 98, 110, 113, 116}
   The result is a block of 80 coded bits, {hc(0), hc(1), ... , hc(79)}
   MCS5-6 Downlink
   A spare bit is added at the end of this block:
   hc(k) = C(k) for k = 0, 1, ... , 98
   hc(99) = C(98)
   The result is a block of 100 coded bits, {hc(0), hc(1), ... , hc(99)}.
   MCS5-6 Uplink
   The code is punctured in such a way that the following coded bits:
   hc(k) = C(k) for k = 0, 1, ..., 134
   hc(135) = C(134)
   The result is a block of 136 coded bits, {hc(0), hc(1), ... , hc(135)}.
   MCS7-9 Downlink
   The code is punctured in such a way that these coded bits are not transmitted:
   {C(k) for k = 14, 23, 33, 50, 59, 69, 86, 95, 105, 122, 131}

The result is a block of 124 coded bits, {hc(0), hc(1), ... , hc(123)}.

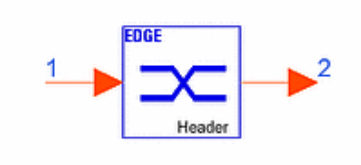
MCS7-9 Uplink

The code is punctured in such a way that these coded bits are not transmitted:
{C(k) for k = 35, 131}
The result is a block of 160 coded bits, {hc(0), hc(1), ... , hc(159)}.

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_HeaderIntrlv



Description Header interleaver
Library EDGE, Channel Coding
Class SDFEDGE_HeaderIntrlv

Parameters

Name	Description	Default	Type
CodingScheme	type of coding scheme: MCS5-6, MCS7-9	MCS5-6	enum
LinkType	type of link: DownLink, UpLink	DownLink	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input data block	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output data block	anytype

Notes/Equations

1. This model is used for interleaving header bits in modulation and coding schemes MCS5 to MCS9.
   Each firing, N output tokens are produced when N input tokens are consumed; refer to N Values.

   N Values

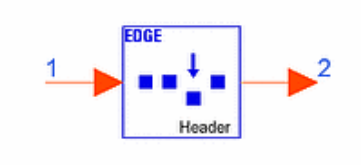
CodingScheme	LinkType	N
MCS5-6	DownLink	100
	UpLink	136
MCS7-9	DownLink	124
	UpLink	160

2. Header Interleaving Rules
   MCS5-6 Downlink
   The 100 coded bits of the header, {hc(0), hc(1), ... , hc(99)}, are interleaved according to:
   hi(j) = hc(k) for k = 0, 1, ... , 99
   j = 25(k mod 4) + ((17k) mod 25)
   MCS5-6 Uplink
   The 136 coded bits of the header, {hc(0), hc(1), ... , hc(135)}, are interleaved according to:
   hi(j) = hc(k) for k = 0, 1, ... , 135
   j == 34(k mod 4) + 2((11k) mod 17) + [(k mod 8)/4]
   MCS7-9 Downlink
   The 124 coded bits of the header, {hc(0), hc(1), ... , hc(123)}, are interleaved according to:
   hi(j) = hc(k) for k = 0, 1, ... , 123
   j == 31(k mod 4) + ((17k) mod 31)
   MCS7-9 Uplink
   The 160 coded bits of the header, {hc(0), hc(1), ... , hc(159)}, are interleaved according to:
   hi(j) = hc(k) for k = 0, 1, ... , 159
   j == 40(k mod 4) + 2((13(k div 8)) mod 20) + ((k mod 8) div 4)

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_HeaderPunc



Description Header puncture
Library EDGE, Channel Coding
Class SDFEDGE_HeaderPunc

Parameters

Name	Description	Default	Type
CodingScheme	type of coding scheme: MCS1-4, MCS5-6, MCS7-9	MCS1-4	enum
LinkType	type of link: DownLink, UpLink	DownLink	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input data block	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output data block	anytype

Notes/Equations

1. This model is used for puncturing header bits in modulation and coding schemes MCS1 to MCS9.
   Each firing, OutputLen output tokens are produced when InputLen input tokens are consumed; refer to InputLen and OutputLen Values.

InputLen and OutputLen Values

CodingScheme	LinkType	InputLen	OutputLen
MCS1-4	DownLink	108	68
	UpLink	117	80
MCS5-6	DownLink	99	100
	UpLink	135	136
MCS7-9	DownLink	135	124
	UpLink	162	160

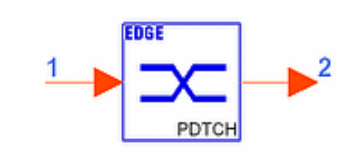
2. Header Puncturing Rules
   MCS1-4 Downlink
   The code is punctured in such a way that these coded bits are not transmitted:
   {C(2+3j) for j = 0, 1, ... , 35} as well as {C(k) for k = 34, 58, 82, 106}
   The result is a block of 68 coded bits, {hc(0), hc(1), ... , hc(67)}.
   MCS1-4 Uplink
   The code is punctured in such a way that these coded bits are not transmitted:
   {C(5+12j), C(8+12j), C(11+12j), for j = 0, 1, ... , 8} as well as {C(k) for k = 26, 38, 50, 62, 74, 86, 98, 110, 113, 116}
   The result is a block of 80 coded bits, {hc(0), hc(1), ... , hc(79)}.
   MCS5-6 Downlink
   A spare bit is added at the end of this block:
   hc(k) = C(k) for k = 0, 1, ... , 98
   hc(99) = C(98)
   The result is a block of 100 coded bits, {hc(0), hc(1), ... , hc(99)}.
   MCS5-6 Uplink
   A spare bit is added at the end of this block:
   hc(k) = C(k) for k = 0, 1, ... , 134
   hc(135) = C(134)
   The result is a block of 136 coded bits, {hc(0), hc(1), ... , hc(135)}.
   MCS7-9 Downlink
   The code is punctured in such a way that these coded bits are not transmitted:
   {C(k) for k = 14, 23, 33, 50, 59, 69, 86, 95, 105, 122, 131}
   The result is a block of 124 coded bits, {hc(0), hc(1), ... , hc(123)}.
   MCS7-9 Uplink
   The code is punctured in such a way that these coded bits are not transmitted:

{C(k) for k = 35, 131}
The result is a block of 160 coded bits, {hc(0), hc(1), ... , hc(159)}.

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_Interleaver



Description Interleaving for packet data traffic channels
Library EDGE, Channel Coding
Class SDFEDGE_Interleaver

Parameters

Name	Description	Default	Type
CodingScheme	type of coding scheme: CS1-4&MCS1-4, MCS5-6, MCS7, MCS8-9	CS1-4&MCS1-4	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	convolutionally encoded and punctured symbols.	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	output	interleaved symbols.	anytype

Notes/Equations

1. This model is used to accomplish data interleaving for packet data traffic channels of EDGE.
   Input and output data lengths depend on the type of coding scheme:
   - for CS1-4&MCS1-4, 456 symbols are consumed at the input and produced at the output.
   - for MCS5-6, 1248 symbols are consumed at the input and produced at the output.
   - for MCS7 and MCS8-9, 1224 symbols are consumed at input and produced at output.
2. For interleaving rules, the following naming conventions are used.
   - *k* and *j* for numbering of bits in data blocks and bursts
   - *Kx* gives the amount of bits in one block, where *x* refers to data type
   - *n* is used for numbering of delivered data blocks
   - *N* marks a certain data block
   - *B* is used for numbering of bursts or blocks where
   - *B0* marks the first burst or block carrying bits from the data block with *n* = 0 (first data block in the transmission).
   - Data delivered to the encoding unit:
     d(k) for k = 0, 1, ... , Kd-1
   - Data after the first encoding step (block code, cyclic code):
     u(k) for k = 0, 1, ... , Ku-1
   - Data after the second encoding step (convolutional code):
     c(n,k) or c(k) for k = 0, 1, ... , Kc-1
     n = 0, 1, ... , N, N+1, ...
   - Interleaved data:
     i(B,k) for k = 0, 1, ... , Ki-1
     B = B0, B0+1, ...
     CS1-4 Interleaving Rules
     i(B,j) = c(n,k) for k = 0, 1, ... , 455
     n = 0, 1, ... , N, N+1, ...
     $B = B_{0 + 4n + (k \bmod 4)}$
     $j = 2((49k) \bmod 57) + ((k \bmod 8) \operatorname{div} 4)$
     MCS1-4 Downlink Interleaving Rules
     The USF, header and data are combined as one entity as follows:
     c(k) = u'(k) for k = 0, 1, ... , 11
     c(k) = hc(k-12) for k = 12, 13, ... , 79
     c(k) = dc(k-80) for k = 80, 81, ... , 451
     c'(n,k) = c(n,k) for k = 0, 1, ... , 24
     c'(n,k) = c(n,k-1) for k = 26, 27, ... , 81
     c'(n,k) = c(n,k-2) for k = 83, 84, ... , 138
     c'(n,k) = c(n,k-3) for k = 140, 141, ... , 423
     c'(n,k) = c(n,k-4) for k = 425, 426, ... , 455
     c'(n,25) = q(8); c'(n,82) = q(9); c'(n,139) = q(10); c'(n,424) = q(11);
     c(n,k) are the coded bits and q(8), q(9), ..., q(11) = 0,0,0,0 are four extra

stealing flags
The resulting block is interleaved according to the following rule:
i(B,j) = c'(n,k) for k = 0, 1, ... , 455
n = 0, 1, ... , N, N+1, ...
B = B0 + 4n + (k mod 4)
j = 2((49k) mod 57) + ((k mod 8) div 4)

MCS1-4 Uplink Interleaving Rules

The header and data are combined as one entity as follows:
c(k) = hc(k) for k = 0, 1, ... , 79
c(k) = dc(k-80) for k = 80, 81, ... , 451
c'(n,k) = c(n,k) for k = 0, 1, ... , 24
c'(n,k) = c(n,k-1) for k = 26, 27, ... , 81
c'(n,k) = c(n,k-2) for k = 83, 84, ... , 138
c'(n,k) = c(n,k-3) for k = 140, 141, ... , 423
c'(n,k) = c(n,k-4) for k = 425, 426, ... , 455
c'(n,25) = q(8); c'(n,82) = q(9); c'(n,10) = q(2); c'(n,424) = q(11);
c(n,k) are the coded bits and q(8), q(9), ..., q(11) = 0, 0, 0, 0 are four extra stealing flags
The resulting block is interleaved according to:
i(B,j) = c'(n,k) for k = 0, 1, ... , 455
n = 0, 1, ... , N, N+1, ...
B = B0 + 4n + (k mod 4)
j = 2((49k) mod 57) + ((k mod 8) div 4)

MCS5-6 Downlink and Uplink Interleaving Rules

There is no closed expression describing the interleaver, but it has been derived as follows.

- A block interleaver with a 1392 bit block size is defined:
  The kth input data bit is mapped to the jth bit of the Bth burst, where
  k = 0, ... , 1391
  B = mod(k,4)
  d = mod(k,464)
  j = 3*(2mod(25d,58) + div(mod(d,8),4) + 2(-1)Bdiv(d,232)) + mod(k,3)
- Data bit positions being mapped onto header positions in the interleaved block are removed (header positions are j = 156, 157, ... , 191) when the header is placed next to the training sequence. This leaves 1248 bits in the mapping.
- The bits are renumbered to fill the gaps in j and k without changing the relative order.
  The resulting interleaver transforms the block of 1248 coded bits, {dc(0), dc(1), ... , dc(1247)} into a block of 1248 interleaved bits, {di(0), di(1), ... , di(1247)}.
  di(j) = dc(k) for k = 0, 1, ... , 1247
  An explicit relation between j and k is given in table 15 in reference[1]; interleaving of MCS5 and MCS6 in this model is based on this table.

MCS7 Downlink and Uplink Interleaving Rules

Data is combined as one entity:
dc(k) = c1(k) for k = 0, 1, ... , 611
dc(k) = c2(k-612) for k = 612, 613, ... , 1223
The resulting block is interleaved:
di(j) = dc(k)for k = 0, 1, ... , 1223
j = 306(k mod 4) + 3((44k) mod 102 + (k div 4) mod 2) + (k + 2 - (k div 408)) mod 3

MCS8-9 Downlink and Uplink Interleaving Rules

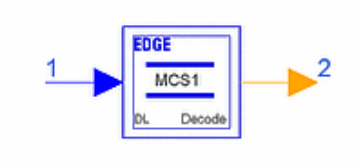
Data is combined as one entity:
dc(k) = c1(k) for k = 0, 1, ... , 611
dc(k) = c2(k-612) for k = 612, 613, ... , 1223

The resulting block is interleaved:
di(j) = dc(k) for k = 0, 1, ... , 1223
j = 306(2(k div 612) + (k mod 2) + 3((74k) mod 102 + (k div 2) mod 2) + (k + 2 - (k div 204)) mod 3

References

1. ETSI SMG2 EDGE Tdoc 999/99, CR 05.03-A025 EGPRS Channel Coding, Bordeaux, France, September 20-24, 1999.
2. ETSI SMG2 EDGE Tdoc 278/99, EGPRS Channel Coding, Paris, France, 24-27 August 1999.

EDGE_MCS1_DL_Decoder



Description MCS1 decoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS1_DL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

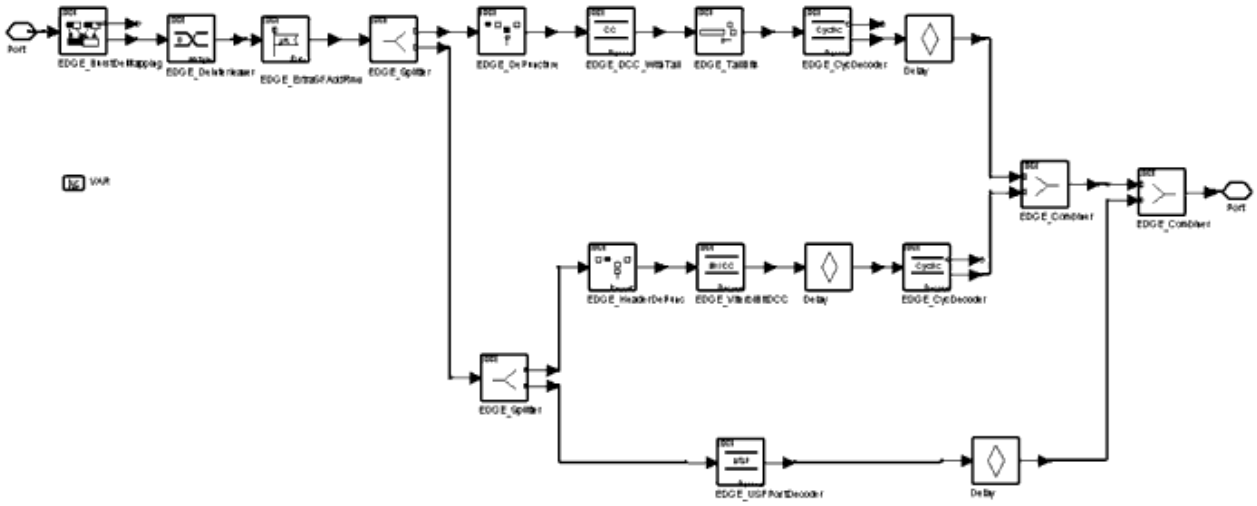
Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of downlink coding scheme MCS1. The output has a delay of 209 bits.
2. The schematic for this subnetwork is shown in the figure below. It consists of splitters, combiners, burst de-mapping, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, cyclic code decoders, and a USF post decoder.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (that is, 5 × 7 = 35 bits here), the output will have a delay of one data block, 209 bits.
   The number of data blocks of delay can be determined by the equation
   $$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$
   where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
   For details regarding the MCS1 downlink, refer to [1].



EDGE_MCS1_DL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24,

1999.

EDGE_MCS1_DL_Encoder

Description MCS1 encoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS1_DL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

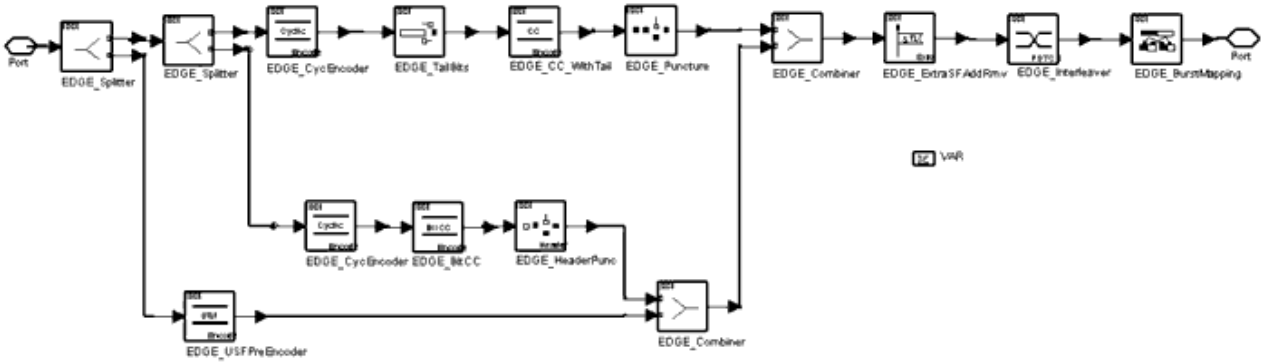
Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS1 in a downlink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a USF pre-coder, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, an interleaver and a burst mapping.

For details regarding the MCS1 downlink, refer to Reference 1.

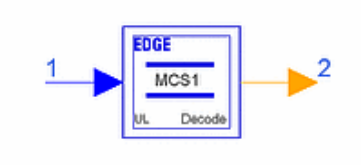


EDGE_MCS1_DL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS1_UL_Decoder



Description MCS1 decoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS1_UL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

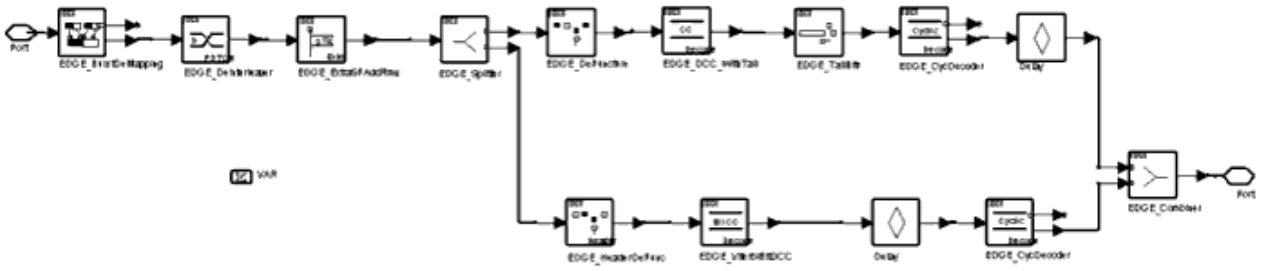
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS1 in an uplink. The output has a delay of 209 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a burst de-mapping, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, and cyclic code decoders.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length, i.e. 5 × 7 = 35 bits here, the output will have a delay of one data block, i.e. 209 bits. The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS1 uplink, refer to Reference 1.



EDGE_MCS1_UL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS1_UL_Encoder

Description MCS1 encoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS1_UL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

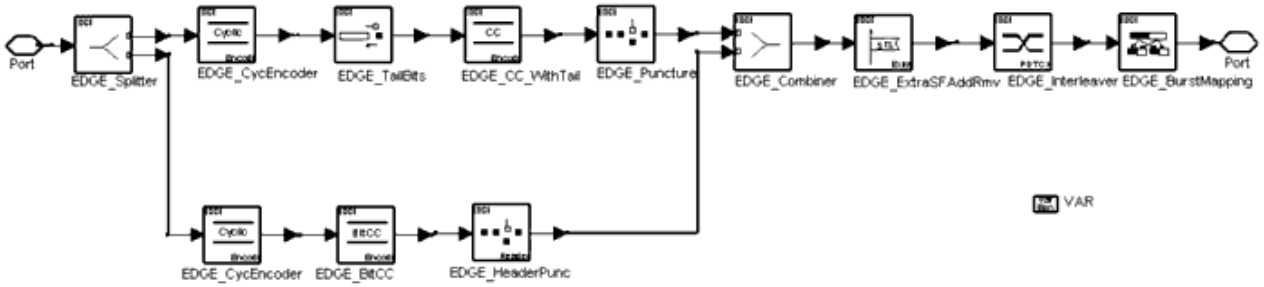
Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS1 in an uplink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, an interleaver and a burst mapping.

For details regarding the MCS1 uplink, see Reference 1.



EDGE_MCS1_UL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS2_DL_Decoder

Description MCS2 decoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS2_DL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

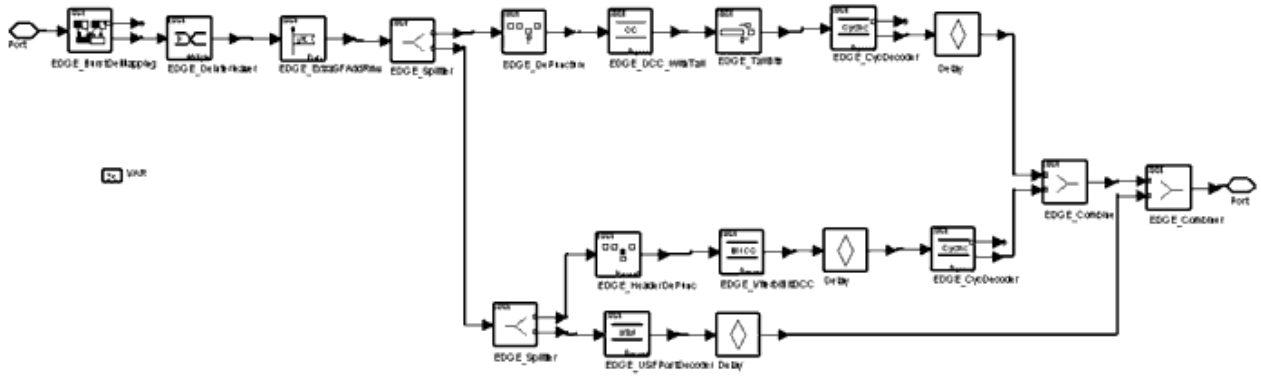
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS2 in a downlink. The output has a delay of 257 bits.
2. The schematic for this subnetwork is shown in the following diagram. It consists of splitters, combiners, a burst de-mapping, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, cyclic code decoders and a USF post decoder.
3. Because the viterbi decoder of header bits has a delay of five times constraint length, i.e. 5 × 7 = 35 bits here, the output will have a delay of one data block, i.e. 257 bits. The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS2 downlink, see Reference 1.



EDGE_MCS2_DL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS2_DL_Encoder

Description MCS2 encoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS2_DL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

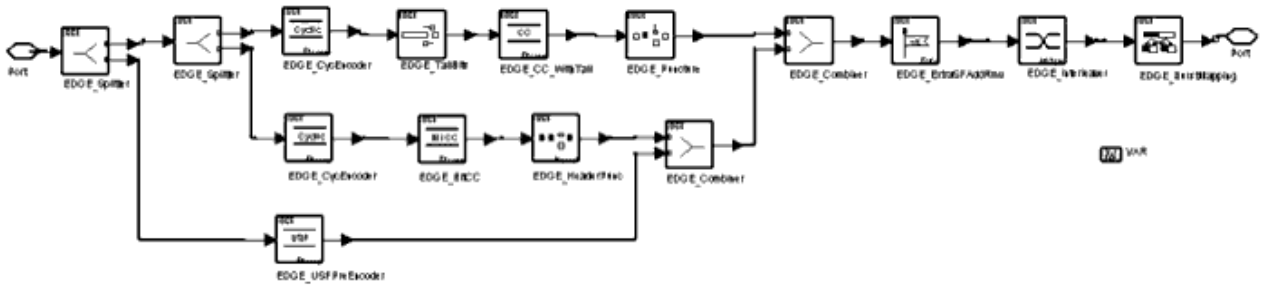
Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS2 in a downlink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a USF pre-coder, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, an interleaver and a burst mapping.

For details regarding the MCS2 downlink, see Reference 1.

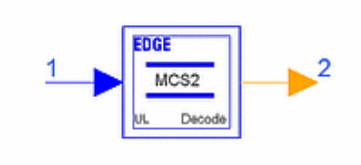


EDGE_MCS2_DL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS2_UL_Decoder



Description MCS2 decoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS2_UL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

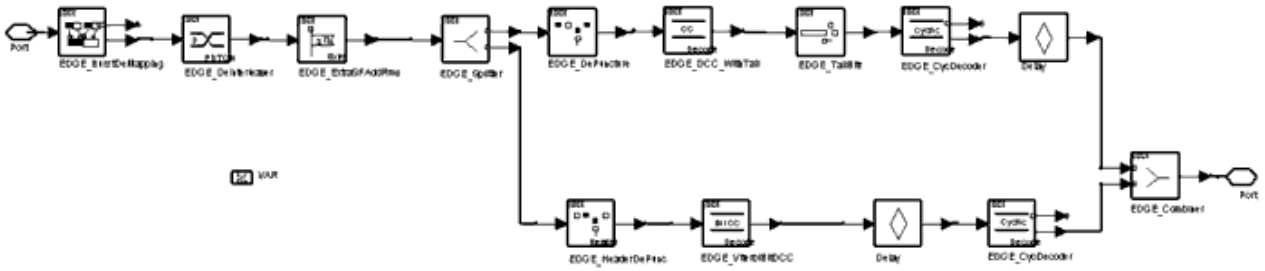
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS2 in an uplink. The output has a delay of 257 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a burst de-mapping, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, and cyclic code decoders.
3. Because the viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits) the output will have a delay of one data block (257 bits). The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS2 uplink, refer to Reference 1.



EDGE_MCS2_UL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS2_UL_Encoder

Description MCS2 encoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS2_UL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

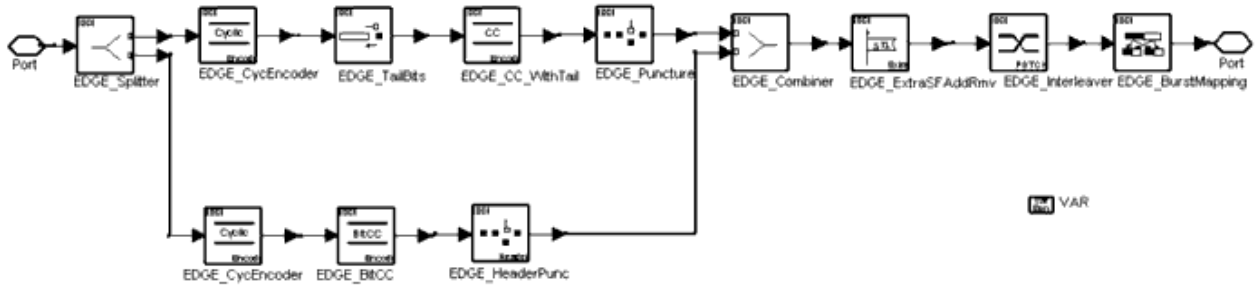
Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS2 in an uplink.
2. The schematic for this subnetwork is shown in the figure below. It consists of splitters, combiners, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, an interleaver, and burst mapping.

For details regarding the MCS2 uplink, see Reference 1.



EDGE_MCS2_UL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS3_DL_Decoder

Description MCS3 decoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS3_DL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

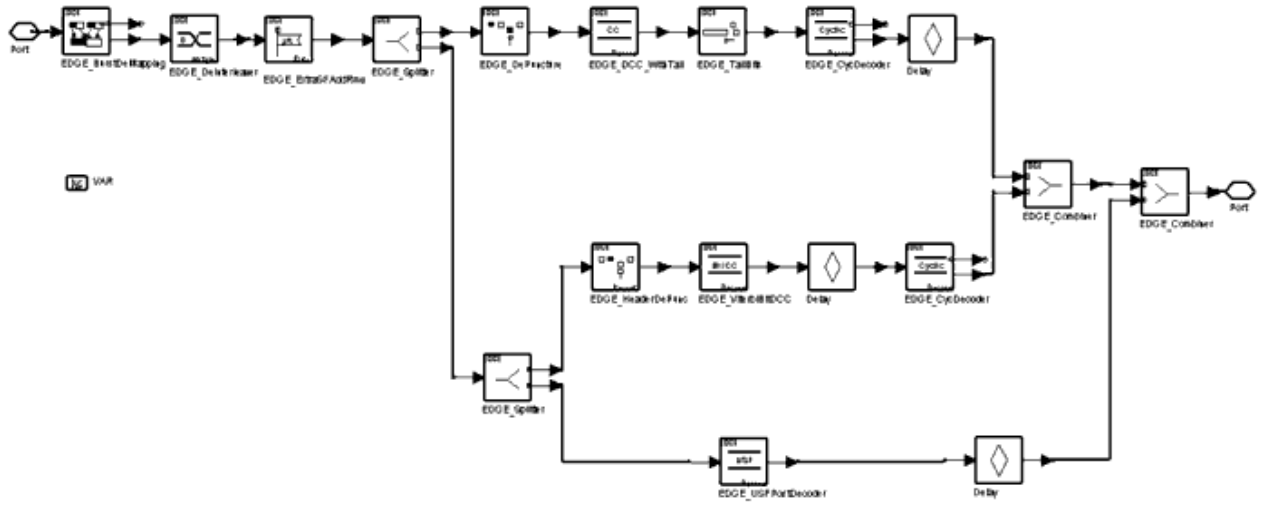
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS3 in a downlink. The output has a delay of 329 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, burst de-mapping, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, cyclic code decoders, and a USF post-decoder.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5×7=35 bits here) the output will have a delay of one data block (329 bits). The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS3 downlink, see Reference 1.



EDGE_MCS3_DL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS3_DL_Encoder

Description MCS3 encoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS3_DL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

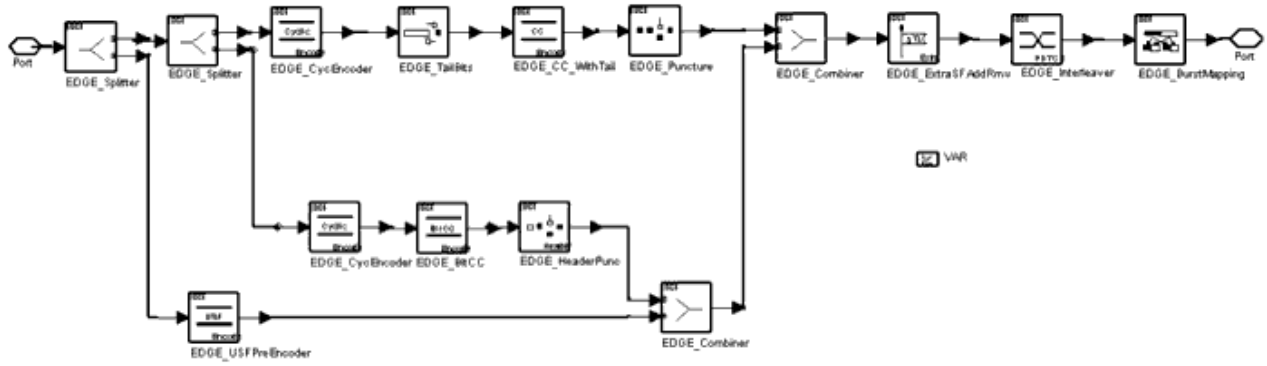
Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS3 in a downlink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a USF pre-coder, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, an interleaver and a burst mapping.
   For details regarding the MCS3 downlink, see Reference 1.

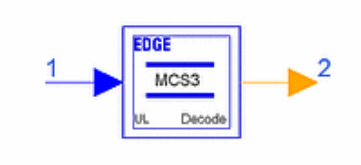


EDGE_MCS3_DL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS3_UL_Decoder



Description MCS3 decoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS3_UL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

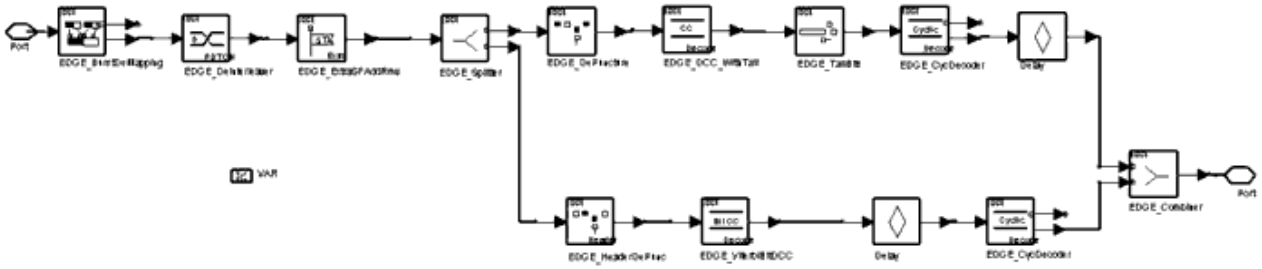
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS3 in an uplink. The output has a delay of 329 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a burst de-mapping, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, and cyclic code decoders.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here) the output will have a delay of one data block (329 bits). The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS3 downlink, refer to Reference 1.



EDGE_MCS3_UL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS3_UL_Encoder

Description MCS3 encoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS3_UL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

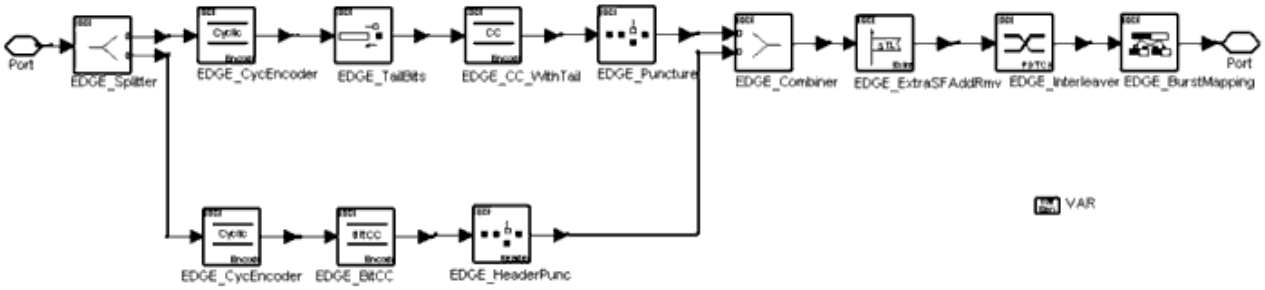
Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS3 in an uplink.
2. The structure of the subnetwork is shown in the following figure. It consists of splitters, combiners, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, an interleaver and, burst mapping.

For details regarding the MCS3 uplink, see Reference 1.



EDGE_MCS3_UL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS4_DL_Decoder

Description MCS4 decoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS4_DL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

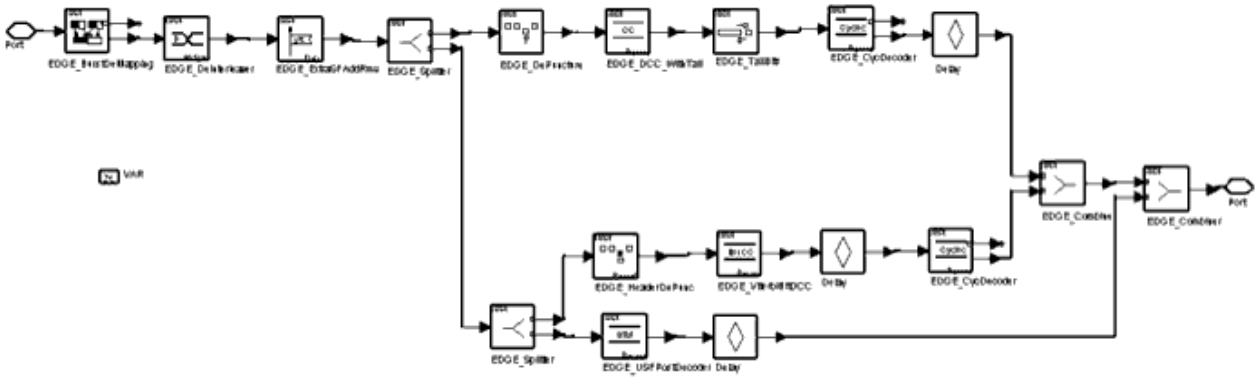
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS4 in a downlink. The output has a delay of 385 bits.
2. The structure of the subnetwork is shown in the following figure. It consists of splitters, combiners, burst de-mapping, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, cyclic code decoders, and a USF post-decoder.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here) the output will have a delay of one data block (385 bits). The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS4 downlink, see Reference 1.



EDGE_MCS4_DL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS4_DL_Encoder

Description MCS4 encoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS4_DL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

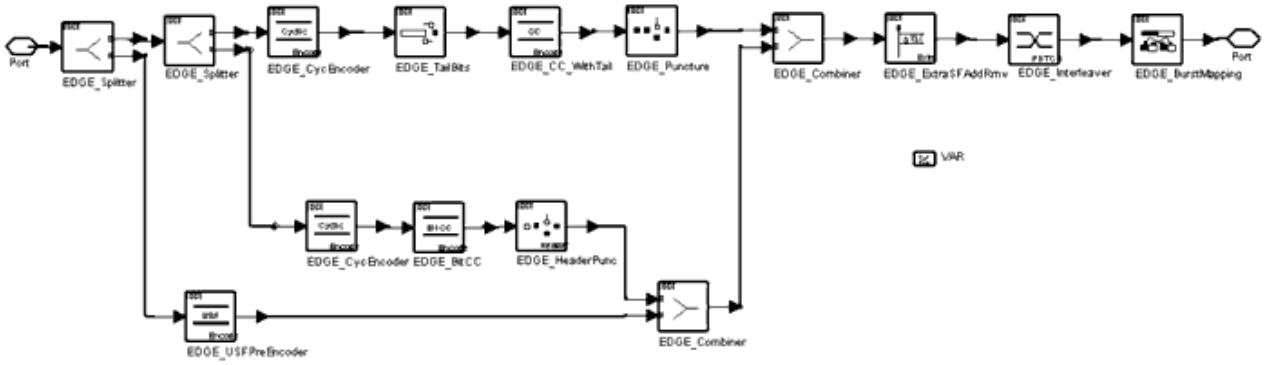
Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used to implement channel encoding of coding scheme MCS4 in a downlink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a USF pre-coder, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, an interleaver, and burst mapping.

For details regarding the MCS4 downlink, refer to Reference 1.

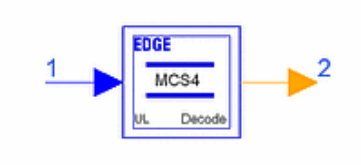


EDGE_MCS4_DL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, 20-24 September 1999.

EDGE_MCS4_UL_Decoder



Description MCS4 decoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS4_UL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

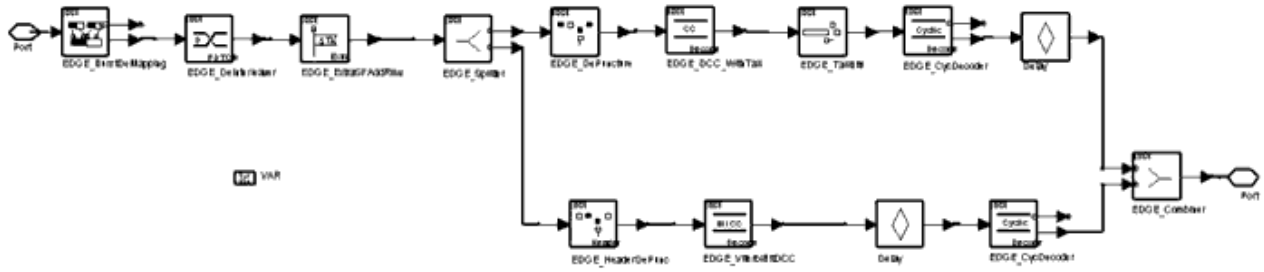
Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS4 in an uplink. The output has a delay of 385 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, burst de-mapping, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, and cyclic code decoders.
   Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here), the output will have a delay of one data block (385 bits).
   The number of data blocks of delay can be determined by the equation
   $$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor 1$$
   where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
   For details regarding the MCS4 uplink, see Reference 1.



EDGE_MCS4_UL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS4_UL_Encoder

Description MCS4 encoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS4_UL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

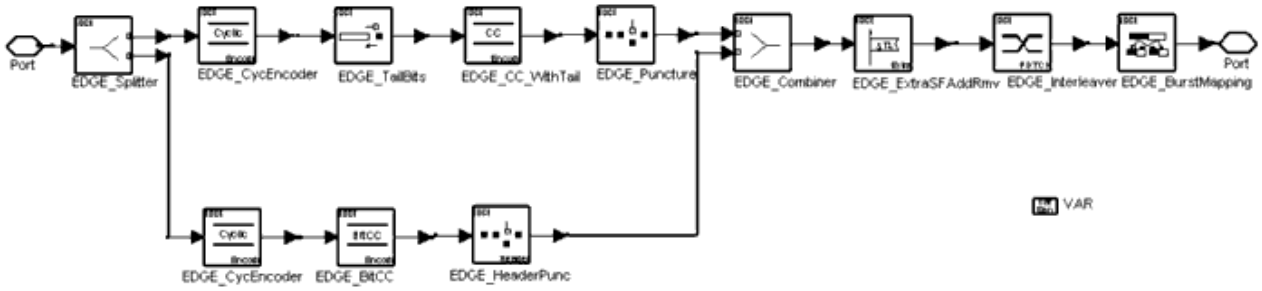
Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS4 in an uplink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, an interleaver, and burst mapping.

For details regarding the MCS4 uplink, refer to Reference 1.



EDGE_MCS4_UL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS5_DL_Decoder

Description MCS5 decoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS5_DL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

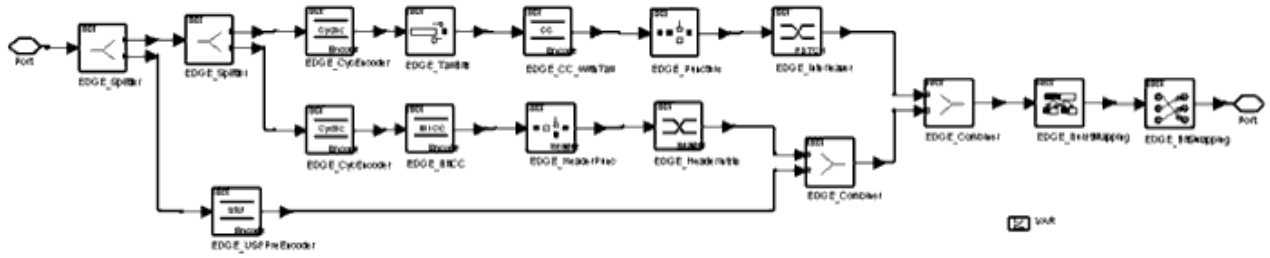
Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS5 in a downlink. The output has a delay of 956 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, bit de-swapping, burst de-mapping, a header de-interleaver, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, cyclic code decoders, and a USF post-decoder.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here) and the sum of header and parity bits is less than 35, the output will have a delay of two data blocks (2 × 478 = 956 bits).
   The number of data blocks of delay can be determined by the equation
   $$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$
   where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
   For details regarding the MCS5 downlink, refer to Reference 1.

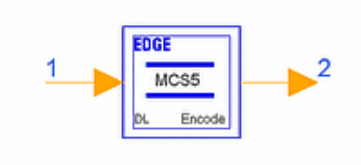


EDGE_MCS5_DL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS5_DL_Encoder



Description MCS5 encoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS5_DL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

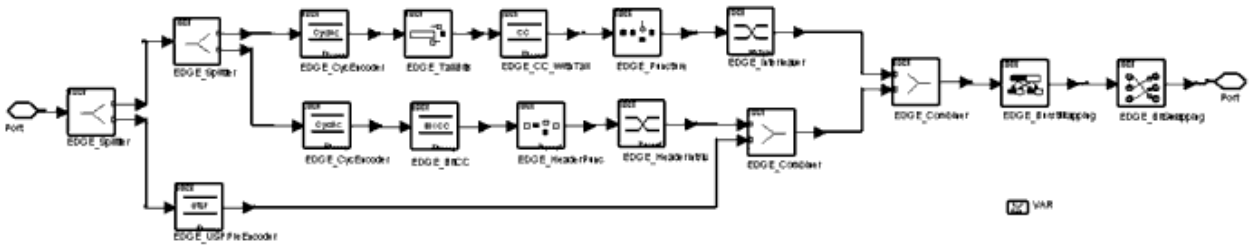
Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS5 in a downlink.
2. The schematic for this subnetwork is shown in the following diagram. It consists of splitters, combiners, a USF pre-coder, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, a header interleaver, an interleaver, burst mapping, and bit swapping.

For details regarding the MCS5 downlink, refer to Reference 1.

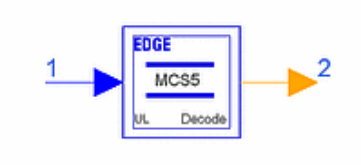


EDGE_MCS5_DL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS5_UL_Decoder



Description MCS5 decoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS5_UL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

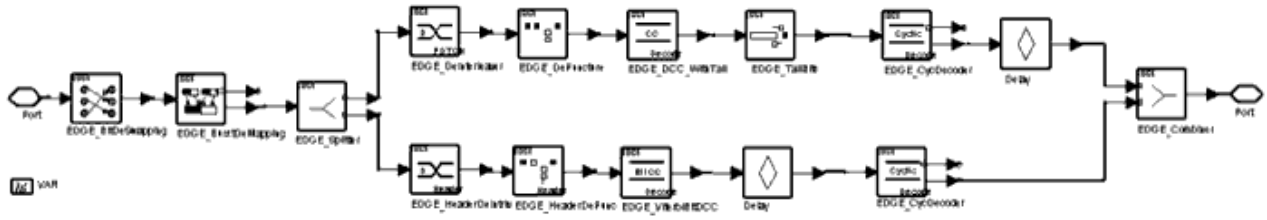
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS5 in an uplink. The output has a delay of 487 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a bit de-swapping, a burst de-mapping, a header de-interleaver, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, and cyclic code decoders.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here) the output will have a delay of one data block (487 bits). The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS5 uplink, see Reference 1.



EDGE_MCS5_UL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS5_UL_Encoder

Description MCS5 encoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS5_UL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

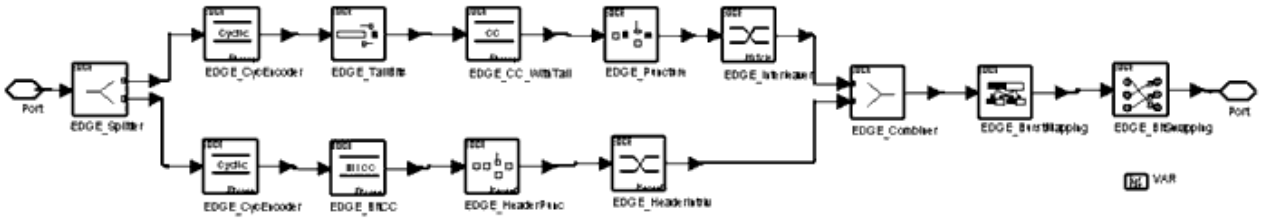
Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS5 in an uplink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, a header interleaver, an interleaver, burst mapping, and bit swapping.

For details regarding the MCS5 uplink, refer to Reference 1.



EDGE_MCS5_UL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS6_DL_Decoder

Description MCS6 decoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS6_DL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

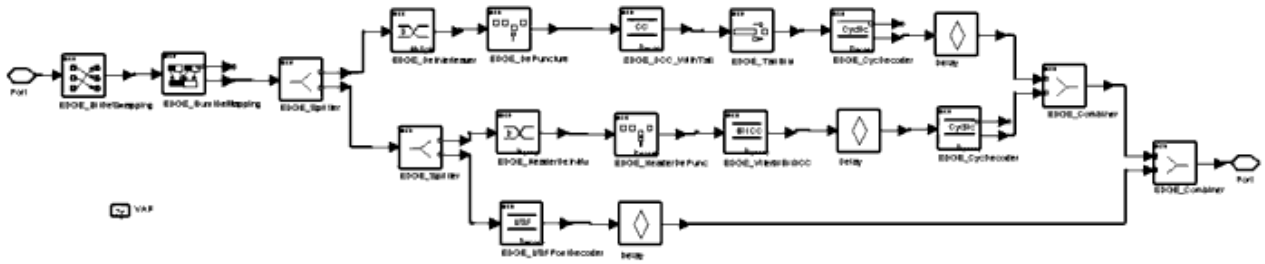
Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS6 in a downlink. The output has a delay of 1244 bits.
2. The schematic for this subnetwork is shown in the following diagram. It consists of splitters, combiners, bit de-swapping, burst de-mapping, a header de-interleaver, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, cyclic code decoders, and a USF post-decoder.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here) and sum of header and parity bits is less than 35, the output will have a delay of two data blocks (2 × 622 = 1244 bits).
   The number of data blocks of delay can be determined by the equation
   $$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$
   where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
   For details regarding the MCS6 downlink, see Reference 1.



EDGE_MCS6_DL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS6_DL_Encoder

Description MCS6 encoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS6_DL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

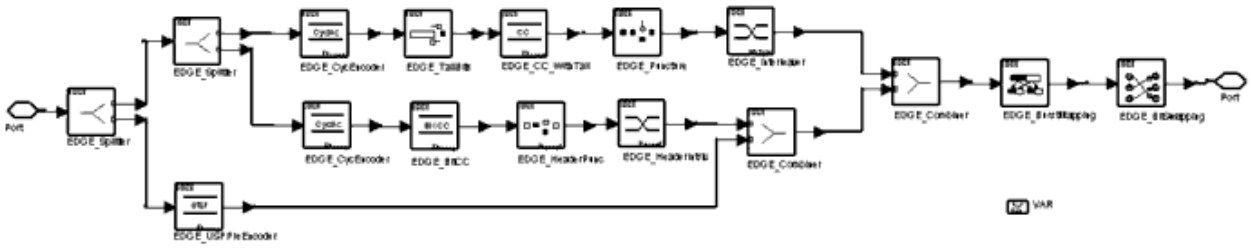
Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS6 in a downlink.
2. The schematic for this subnetwork is shown in the following diagram. It consists of splitters, combiners, a USF pre-coder, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, a header interleaver, an interleaver, burst mapping, and bit swapping. For details regarding the MCS6 downlink, see Reference 1.

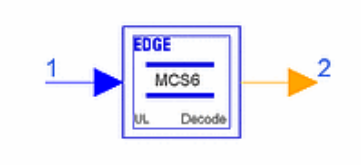


EDGE_MCS6_DL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS6_UL_Decoder



Description MCS6 decoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS6_UL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

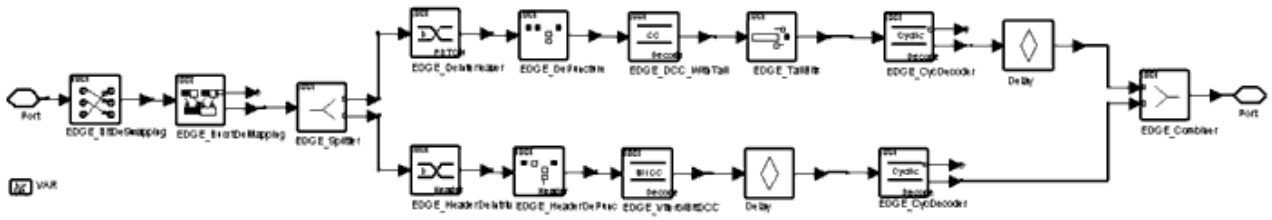
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS6 in an uplink. The output has a delay of 631 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a bit de-swapping, a burst de-mapping, a header de-interleaver, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, and cyclic code decoders.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here), the output will have a delay of one data block (631 bits). The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS6 uplink, see Reference 1.



EDGE_MCS6_UL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS6_UL_Encoder

Description MCS6 encoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS6_UL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2	P1	enum

Pin Inputs

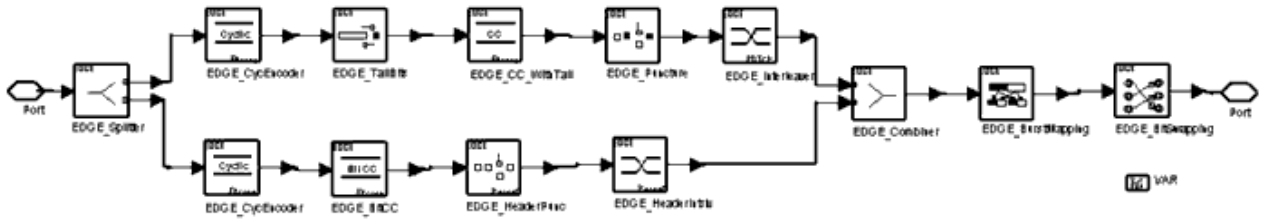
Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS6 in an uplink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, a header interleaver, an interleaver, burst mapping, and bit swapping.
   For details regarding the MCS6 uplink, see Reference 1.

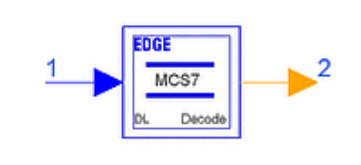


EDGE_MCS6_UL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS7_DL_Decoder



Description MCS7 decoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS7_DL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

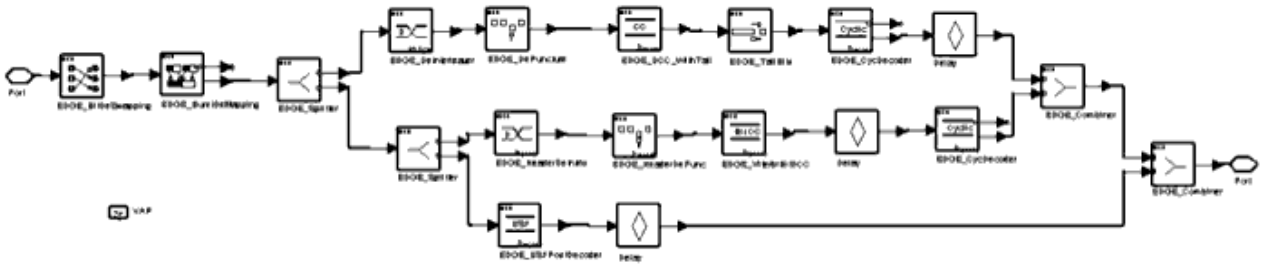
Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS7 in a downlink. The output has a delay of 940 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, bit de-swapping, burst de-mapping, a header de-interleaver, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, cyclic code decoders. and a USF post-decoder.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here), and the sum of header and parity bits is less than 35, the output will have a delay of one data block (940 bits).
   The number of data blocks of delay can be determined by the equation
   $$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$
   where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
   For details regarding the MCS7 downlink, see Reference 1.



EDGE_MCS7_DL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS7_DL_Encoder

Description MCS7 encoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS7_DL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

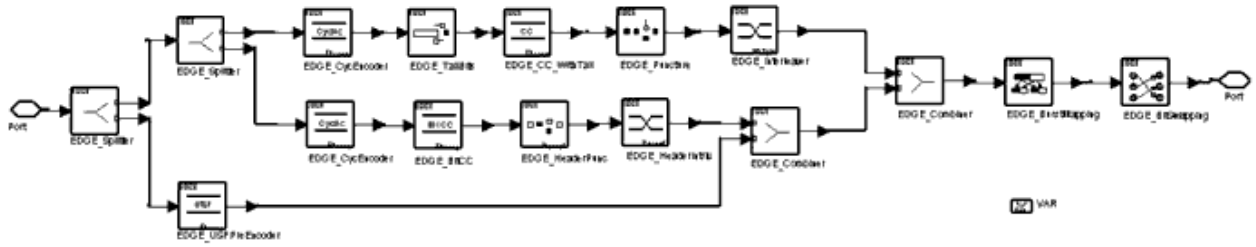
Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS7 in a downlink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a USF pre-coder, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, a header interleaver, an interleaver, burst mapping, and bit swapping. For details regarding the MCS7 downlink, see Reference 1.

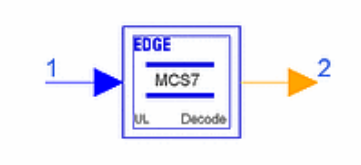


EDGE_MCS7_DL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS7_UL_Decoder



Description MCS7 decoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS7_UL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

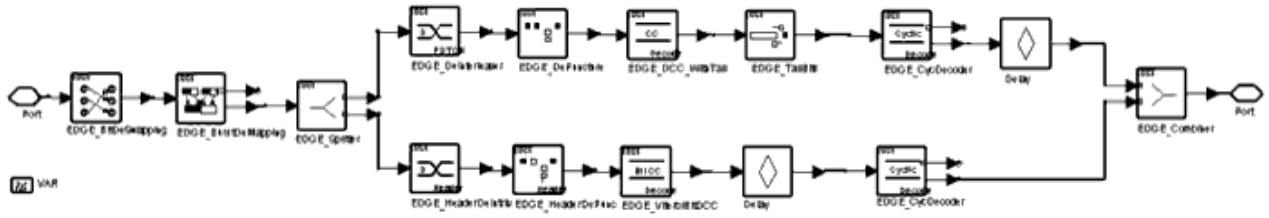
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS7 in an uplink. The output has a delay of 946 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, bit de-swapping, burst de-mapping, a header de-interleaver, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, and cyclic code decoders.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here) the output will have a delay of one data block (946 bits). The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS7 uplink, see Reference 1.



EDGE_MCS7_UL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS7_UL_Encoder

Description MCS7 encoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS7_UL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

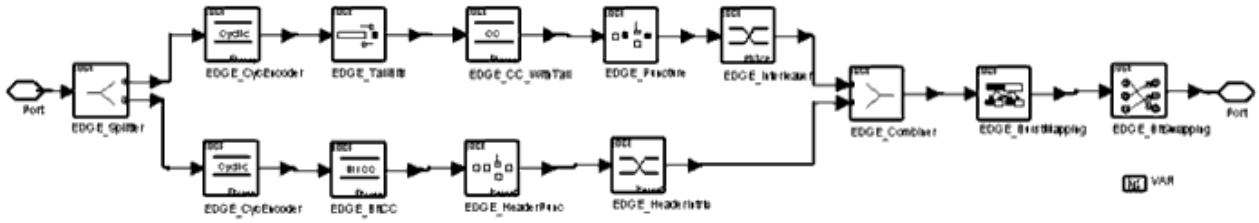
Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS7 in an uplink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, a header interleaver, an interleaver, burst mapping, and bit swapping.
   For details regarding the MCS7 uplink, see Reference 1.

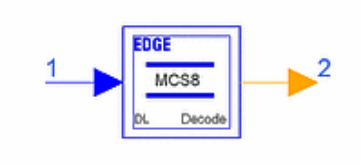


EDGE_MCS7_UL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS8_DL_Decoder



Description MCS8 decoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS8_DL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

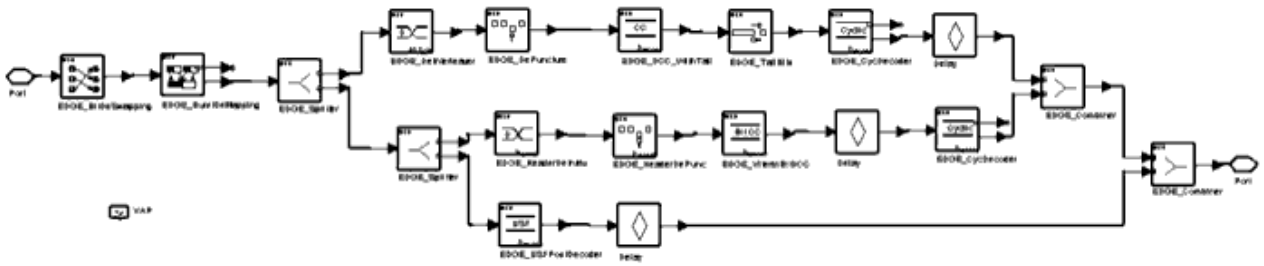
Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS8 in a downlink. The output has a delay of 1132 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, bit de-swapping, burst de-mapping, a header de-interleaver, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, cyclic code decoders, and a USF post-decoder.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here) and the sum of header and parity bits is less than 35, the output will have a delay of one data block (1132 bits).
   The number of data blocks of delay can be determined by the equation
   $$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$
   where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
   For details regarding the MCS8 downlink, see Reference 1.



EDGE_MCS8_DL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS8_DL_Encoder

Description MCS8 encoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS8_DL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

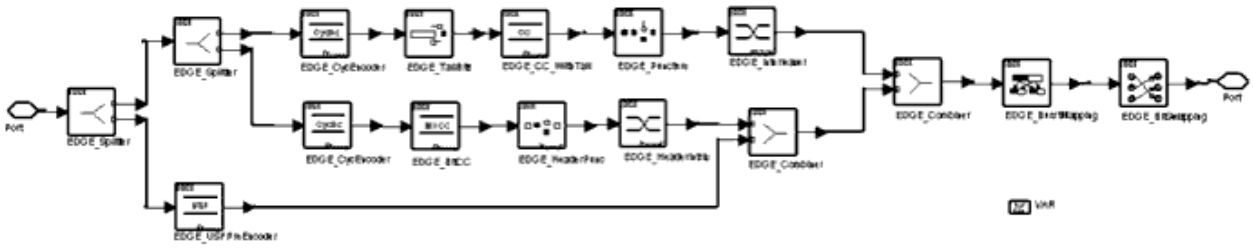
Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS8 in a downlink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a USF pre-coder, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, a header interleaver, an interleaver, burst mapping, and bit swapping. For details regarding the MCS8 downlink, see Reference 1.

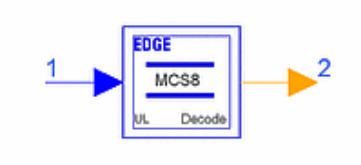


EDGE_MCS8_DL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS8_UL_Decoder



Description MCS8 decoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS8_UL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

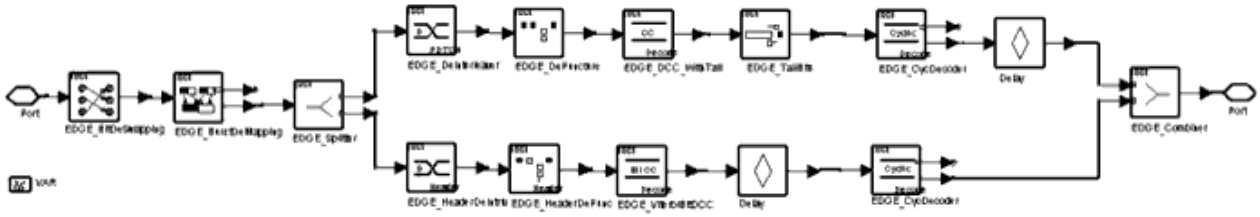
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS8 in an uplink. The output has a delay of 1138 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, bit de-swapping, burst de-mapping, a header de-interleaver, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, and cyclic code decoders.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here), the output will have a delay of one data block (1138 bits). The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS8 uplink, see Reference 1.



EDGE_MCS8_UL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS8_UL_Encoder

Description MCS8 encoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS8_UL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

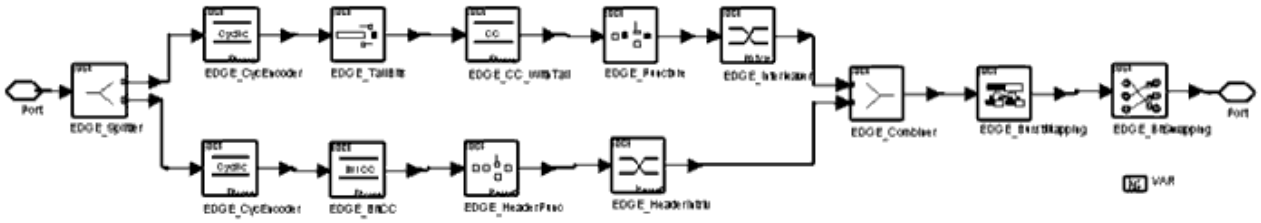
Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS8 in an uplink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, a header interleaver, an interleaver, burst mapping. and bit swapping.
   For details regarding the MCS8 uplink, see Reference 1.

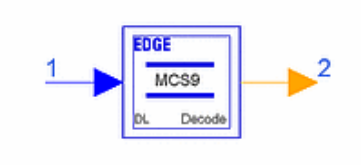


EDGE_MCS8_UL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS9_DL_Decoder



Description MCS9 decoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS9_DL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

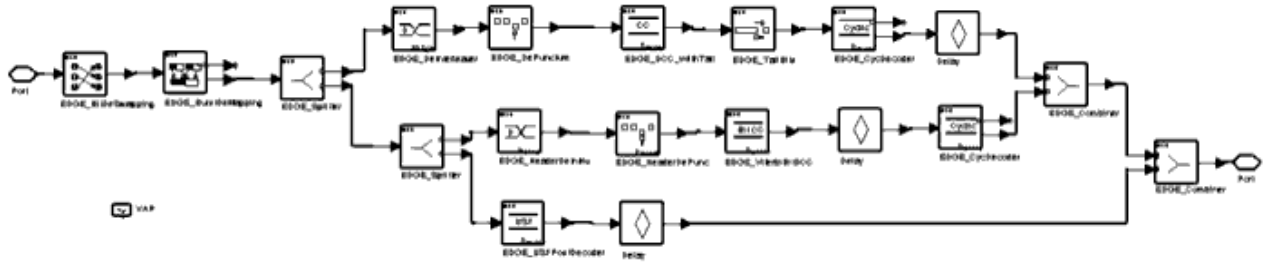
Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS9 in a downlink. The output has a delay of 1228 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, bit de-swapping, burst de-mapping, a header de-interleaver, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, cyclic code decoders, and a USF post-decoder.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here) and the sum of header and parity bits is less than 35, the output will have a delay of one data block (1228 bits).
   The number of data blocks of delay can be determined by the equation
   $$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$
   where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
   For details regarding the MCS9 downlink, see Reference 1.



EDGE_MCS9_DL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS9_DL_Encoder

Description MCS9 encoder for downlink
Library EDGE, Channel Coding
Class SDFEDGE_MCS9_DL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

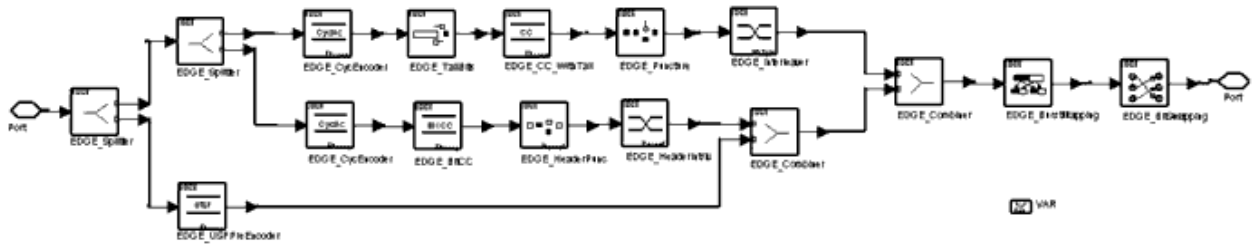
Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS9 in a downlink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, a USF pre-coder, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, a header interleaver, an interleaver, burst mapping, and bit swapping. For details regarding the MCS9 downlink, see Reference 1.

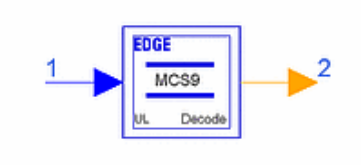


EDGE_MCS9_DL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS9_UL_Decoder



Description MCS9 decoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS9_UL_Decoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	bits to be decoded	real

Pin Outputs

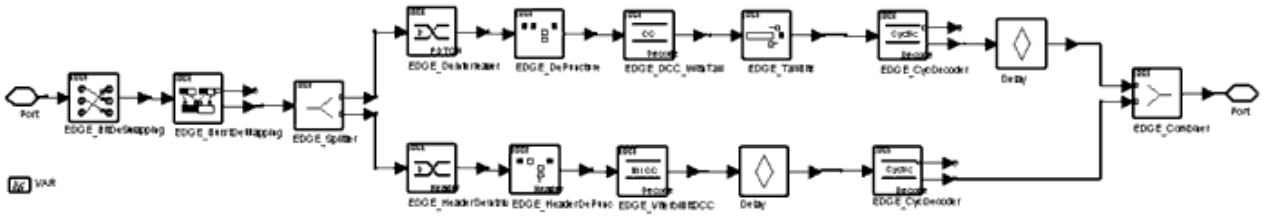
Pin	Name	Description	Signal Type
2	output	information bits decoded	int

Notes/Equations

1. This subnetwork is used for channel decoding of coding scheme MCS9 in an uplink. The output has a delay of 1234 bits.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, bit de-swapping, burst de-mapping, a header de-interleaver, a de-interleaver, an extra stealing flag remover, a de-puncturer, a header de-puncturer, convolutional code decoders, a tail bits remover, and cyclic code decoders.
3. Because the Viterbi decoder of header bits has a delay of five times constraint length (5 × 7 = 35 bits here) the output will have a delay of one data block (1234 bits). The number of data blocks of delay can be determined by the equation

$$N_B = \left\lfloor \frac{5 \times K}{N_H + N_P} \right\rfloor + 1$$

where N_B is the number of data blocks delayed, K is the constraint length of convolutional code, N_H is the number of header bits in a data block, N_P is the number of parity bits added to header bits and $\lfloor x \rfloor$ is the largest integer number that is not greater than x.
For details regarding the MCS9 uplink, see Reference 1.



EDGE_MCS9_UL_Decoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MCS9_UL_Encoder

Description MCS9 encoder for uplink
Library EDGE, Channel Coding
Class SDFEDGE_MCS9_UL_Encoder

Parameters

Name	Description	Default	Type
PuncScheme	puncturing scheme: P1, P2, P3	P1	enum

Pin Inputs

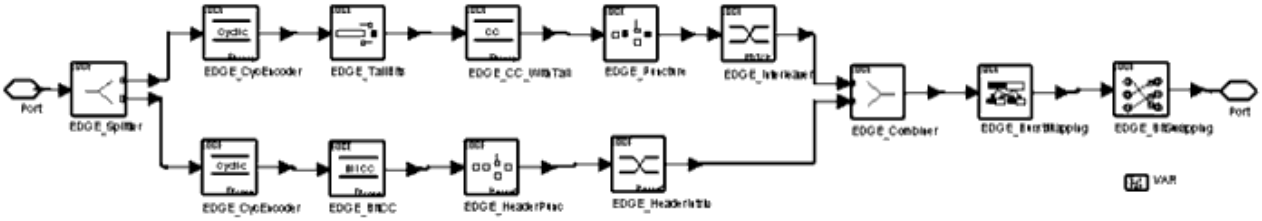
Pin	Name	Description	Signal Type
1	input	input bits to be encoded	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encoded bits	int

Notes/Equations

1. This subnetwork is used for channel encoding of coding scheme MCS9 in an uplink.
2. The schematic for this subnetwork is shown in the following figure. It consists of splitters, combiners, cyclic code encoders, a tail bits inserter, convolutional code encoders, a header puncturer, a puncturer, an extra stealing flags inserter, a header interleaver, an interleaver, burst mapping, and bit swapping.
   For details regarding the MCS9 uplink, see Reference 1.

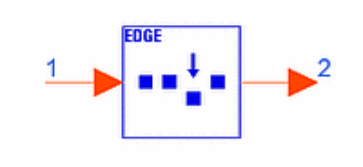


EDGE_MCS9_UL_Encoder Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_Puncture



Description Data puncturing
Library EDGE, Channel Coding
Class SDFEDGE_Puncture

Parameters

Name	Description	Default	Sym	Type	Range
CodingScheme	type of coding scheme: CS_2, CS_3, MCS_1, MCS_2, MCS_3, MCS_4, MCS_5, MCS_6, MCS_7, MCS_8, MCS_9	MCS_1	M	enum	
PuncScheme	puncturing scheme: P1, P2, P3	P1		enum	†
† P1 is the only puncturing scheme for CS2 and CS3 coding schemes; P3 is the only puncturing scheme for MCS3, 4, 7, 8, and 9.					

Pin Inputs

Pin	Name	Description	Signal Type
1	input	convolutionally encoded symbols.	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	output	punctured convolutionally encoded symbols.	anytype

Notes/Equations

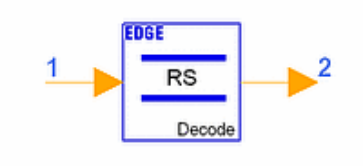
This model is used to puncture convolutionally coded data in each CS and MCS, to attain the desired code rate and carry out the transmitting mode of incremental redundancy. There are no puncturing schemes in CS1 and CS4. Each firing:

- 456 bits are produced at output pin while 588 bits are consumed at input pin, when M = CS_2
- 456 bits are produced at output pin while 676 bits are consumed at input pin, when M = CS_3
- 372 bits are produced at output pin while 588 bits are consumed at input pin, when M = MCS_1
- 372 bits are produced at output pin while 732 bits are consumed at input pin, when M = MCS_2
- 372 bits are produced at output pin while 948 bits are consumed at input pin, when M = MCS_3
- 372 bits are produced at output pin while 1116 bits are consumed at input pin, when M = MCS_4
- 1248 bits are produced at output pin while 1404 bits are consumed at input pin, when M = MCS_5
- 1248 bits are produced at output pin while 1836 bits are consumed at input pin, when M = MCS_6
- 612 bits are produced at output pin while 1404 bits are consumed at input pin, when M = MCS_7
- 612 bits are produced at output pin while 1692 bits are consumed at input pin, when M = MCS_8
- 612 bits are produced at output pin while 1836 bits are consumed at input pin, when M = MCS_9

References

1. ETSI TDOC SMG2 EDGE 999/99, CR 05.03-A025 EGPRS Channel Coding, Bordeaux, France, September 20-24, 1999.
2. ETSI TDOC SMG2 EDGE 278/99, EGPRS Channel Coding, Paris, France, 24-27 August 1999.

EDGE_RSDecoder



Description Reed-Solomon decoder
Library EDGE, Channel Coding
Class SDFEDGE_RSDecoder

Parameters

Name	Description	Default	Sym	Type	Range
GF	Galois Field (2^GF)	8	m	int	[2, 16]
CodeLength	code word length	36	n	int	(2, 2^{m} -1]
InfoLength	information symbol length	32	k	int	(0, n-2]
PrimPolynomial	coefficient of primitive polynomial	1 1 1 0 0 0 0 1 1	p(x)	int array	†
PolynomialRoot	first root of generator polynomial	120	m_0	int	(0, 2^{m} -1 - (n - k)]
† PrimPolynomial must be the coefficients of the m order of polynomial.					

Pin Inputs

Pin	Name	Description	Signal Type
1	in	received symbols for decoding	int

Pin Outputs

Pin	Name	Description	Signal Type
2	out	decoded symbols	int

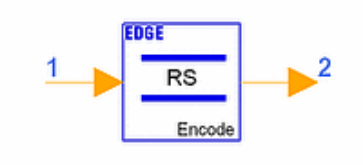
Notes/Equations

1. This model is used to perform RS decoding via the Berlekamp iterative algorithm. The input pin consumes n tokens; the output pin produces k tokens.
2. The Berlekamp iterative algorithm locates the error in RS code and generates an error location polynomial. By finding the root of the error location polynomial, the error position can be determined. If decoding is successful, the information symbols are output; otherwise, the received data is unaltered and the error indicator flag, which is 1, is returned.

References

1. E.R. Berlekamp, Algebraic Coding Theory, McGraw-Hill, New York, 1968.
2. S. Lin and D. J. Costello, Jr., *Error Control Coding Fundamentals and Applications* , Prentice Hall, Englewood Cliffs NJ, 1983.

EDGE_RSEncoder



Description Reed-Solomon encoder
Library EDGE, Channel Coding
Class SDFEDGE_RSEncoder

Parameters

Name	Description	Default	Sym	Type	Range
GF	Galois Field (2^GF).	8	m	int	[2, 16]
CodeLength	code word length.	36	n	int	(2, 2^{m} -1]
InfoLength	information symbol length.	32	k	int	(0, n-2]
PrimPolynomial	coefficient of primitive polynomial.	1 1 1 0 0 0 0 1 1	p(x)	int array	†
PolynomialRoot	first root of generator polynomial.	120	$m_{0\sim}$	int	(0, 2^{m} -1 - (n - k)]
† PrimPolynomial must be the coefficients of the m order of polynomial.					

Pin Inputs

Pin	Name	Description	Signal Type
1	in	information symbols, the input symbols must be in the range [0, 2^m-1]	int

Pin Outputs

Pin	Name	Description	Signal Type
2	out	systematic code words, k information symbols plus n-k parity symbols	int

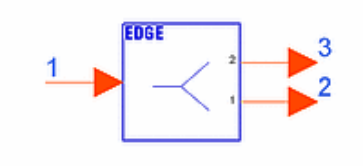
Notes/Equations

1. This model is used to perform Reed-Solomon (RS) encoding. Each firing, k tokens are consumed at input and n tokens are produced at output.
2. RS codes are a class of block codes that operate on non-binary symbols. The symbols are formed from m bits of a binary data stream. A code block is then formed with $n = 2^m - 1$ symbols. In each block, k symbols are formed from the encoder input and $(n-k)$ parity symbols are added. The code is thus a systematic code. The rate of the code is k/n, and the code can correct up to $t = (n-k-1)/2$ or $(n-k)/2$ symbol errors in a block, depending on whether n−k is odd or even. A shortened code can be formed by taking 32 input symbols, padding them out with 219 all-zero symbols to form 251 symbols, then encoding with an RS code (255,251). The 219 fixed symbols are discarded prior to transmission.

References

1. S. Lin and D. J. Costello, Jr., *Error Control Coding Fundamentals and Applications* , Prentice Hall, Englewood Cliffs NJ, 1983.

EDGE_Splitter



Description Block splitter for channel coding
Library EDGE, Channel Coding
Class SDFEDGE_Splitter

Parameters

Name	Description	Default	Sym	Type	Range
Length1	block length of output1	6	N1	int	(0, ∞
Length2	block length of output2	284	N2	int	(0, ∞)
SplitMode	split mode: first part to be output1, first part to be output2, middle part to be output1, middle part to be output2	first part to be output1		enum	

Pin Inputs

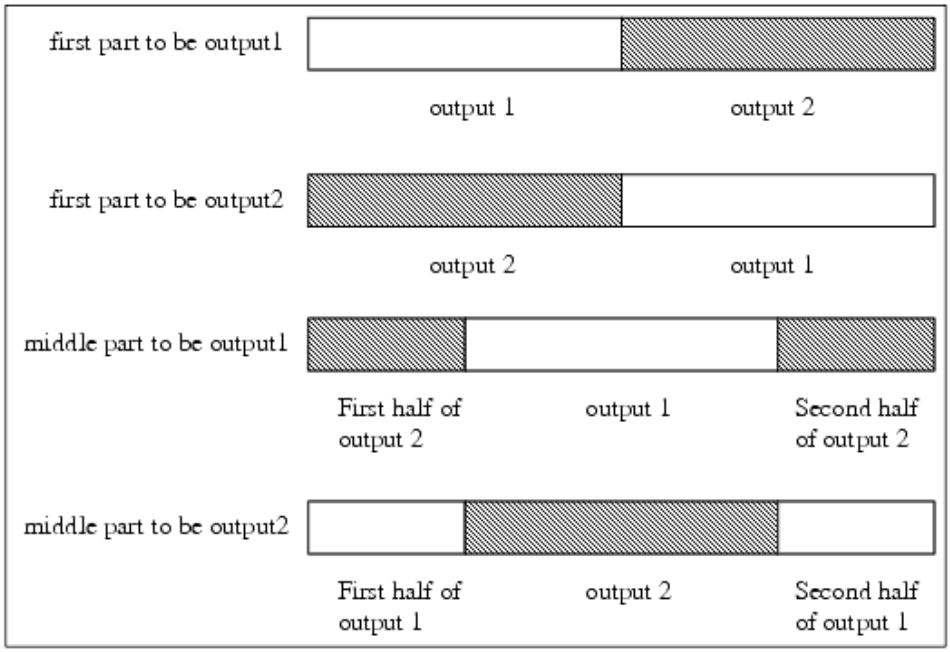
Pin	Name	Description	Signal Type
1	input	input block	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	output1	output block 1	anytype
3	output2	output block 2	anytype

Notes/Equations

1. The model is used to split one input data block into two output data blocks. Each firing, N1 tokens are produced at output1 and N2 tokens are produced at output2 when N1+N2 input tokens are consumed.
2. In EDGE channel coding, different parts of data bits (USF in downlink, header and data) must be split from a data block in a certain way. This model is used to split the input data blocks. To split into three data blocks, two splitters can be used in a cascade.
   The splitting pattern is determined by the SplitMode setting and illustrated in the following figure].
   - When SplitMode = first part to be output1 (or first part to be output2), data of the first half of the input block is output to output1 (or output2), and the other half is output to output2 (or output1).
   - When SplitMode is set to middle part to be output1 (or middle part to be output2), the central half of input block is output to output1 (or output2), and the other parts are output to output2 (or output1).
     When the length of the output block that will be combined from the front and rear parts of the input is odd, the number of bits in the first half will be one less than that of the second half.

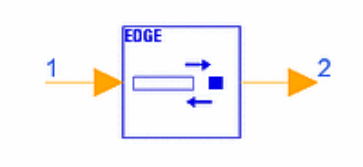


SplitMode Splitting Patterns

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_TailBits



Description Tailing bits adder or remover
Library EDGE, Channel Coding
Class SDFEDGE_TailBits

Parameters

Name	Description	Default	Type	Range
AddRmvSwitch	switch between adding and removing tailing bits: Adding, Removing	Adding	enum	
BitCheck	check range of input bits: Check and stop at error, Check and warn the error, No Check	Check and stop at error	enum	
NumTailBits	number of tailing bits in a frame	4	int	(0, ∞)
InfoLength	number of information bits in a frame	185	int	(0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input frame	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output frame	int

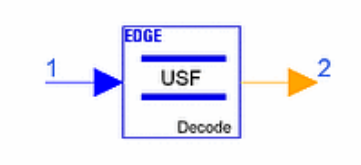
Notes/Equations

1. This model is used to add or remove tailing bits from the input frames. It is used before the convolutional code encoder EDGE_CC_WithTail or after the Viterbi decoder EDGE_DCC_WithTail.
   NumTailBits + InfoLength output tokens are produced for each InfoLength input tokens are consumed when AddRmvSwitch = Adding and InfoLength output tokens are produced for each NumTailBits+InfoLength input tokens consumed when AddRmvSwitch = Removing.
2. If AddRmvSwitch = Adding, NumTailBits are added after every InfoLength; if AddRmvSwitch = Removing, NumTailBits are removed from every NumTailBits+InfoLength input bits.

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.03, "Channel Coding," version 5.1.0, May 1996.

EDGE_USFPostDecoder



Description USF postdecoder
Library EDGE, Channel Coding
Class SDFEDGE_USFPostDecoder

Parameters

Name	Description	Default	Type
CodingScheme	type of coding scheme: CS_2, CS_3, CS_4, MCS_1, MCS_2, MCS_3, MCS_4, MCS_5, MCS_6, MCS_7, MCS_8, MCS_9	CS_2	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input data block	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output data block	int

Notes/Equations

1. This model is used for post-decoding of the three USF-bits in RLC data block. It is used in downlink channel decoding only.
   Each firing, three output tokens are produced when InputLen input tokens are consumed. The value of InputLen depends on the setting of CodingScheme; refer to the first of the following two tables.
2. In channel decoding of downlink PDTCH, the pre-coded USF-bits must be post-decoded into three uncoded USF-bits. The uncoded USF-bits will then be combined with the decoded header and data bits to a RLC data block. In EDGE, three kinds of USF pre-coding schemes are defined; these are listed in the second table.
   Correlation calculation is used in the USF decoding. Input data is correlated with each possible pre-coded bit sequence. When the pre-coded bit sequence that has the maximum correlation value is found, its corresponding uncoded USF bits are output as the decoding results.

CodingScheme	InputLen
CS_2 or CS_3	6
CS_4	12
MCS_5 to MCS_9	36

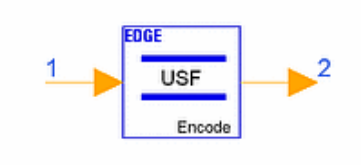
USF Pre-coding Schemes

Channel Coding Scheme	USF Bits	Pre-coded Bits
CS_2 or CS_3	000	000 000
	001	001 011
	010	010 110
	011	011 101
	100	100 101
	101	101 110
	110	110 011
	111	111 000
CS_4MCS_1 to MCS_4	000	000 000 000 000
	001	000 011 011 101
	010	001 101 110 110
	011	001 110 101 011
	100	001 110 101 011
	101	110 111 010 110
	110	111 001 111 101
	111	111 010 100 000
MCS_5 to MCS_9	000	000000000 000000000 000000000 000000000
	001	111110000 111100000 111111000 111110001
	010	111001110 111011100 110000110 110001100
	011	100111100 110000011 101110111 001001111
	100	000110011 001011010 100001101 111111110
	101	110101011 000110101 011101011 100101011
	110	001001101 101111111 011010001 001110100
	111	011010111 010101111 000111110 010010011

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_USFPreEncoder



Description USF pre-encoder
Library EDGE, Channel Coding
Class SDFEDGE_USFPreEncoder

Parameters

Name	Description	Default	Type
CodingScheme	type of coding scheme: CS_2, CS_3, CS_4, MCS_1, MCS_2, MCS_3, MCS_4, MCS_5, MCS_6, MCS_7, MCS_8, MCS_9	CS_2	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input data block	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output data block	int

Notes/Equations

1. This model is used for pre-coding of the 3 USF-bits in RLC data block; it is used in downlink channel coding only.
   Each firing, OutputLen output tokens are produced when three input tokens are consumed. The value of OutputLen depends on the setting of CodingScheme; refer to the first of the following two tables.
2. In channel coding of downlink PDTCH, the first three bits (USF-bits) of the RLC data block is split from the block. These three bits are then pre-coded and combined with the other coded bits. The USF pre-coding schemes are listed in the second table.

CodingScheme	OutputLen
CS_2 or CS_3	6
CS_4	12
MCS_5 to MCS_9	36

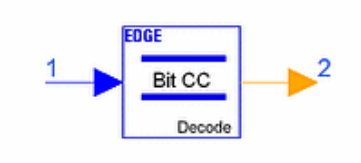
USF Pre-coding Schemes

Channel Coding Scheme	USF bits	Pre-coded bits
CS_2 to CS_3	000	000 000
	001	001 011
	010	010 110
	011	011 101
	100	100 101
	101	101 110
	110	110 011
	111	111 000
CS_4MCS_1 to MCS_4	000	000 000 000 000
	001	000 011 011 101
	010	001 101 110 110
	011	001 110 101 011
	100	001 110 101 011
	101	110 111 010 110
	110	111 001 111 101
	111	111 010 100 000
MCS_5 to MCS_9	000	000000000 000000000 000000000 000000000
	001	111110000 111100000 111111000 111110001
	010	111001110 111011100 110000110 110001100
	011	100111100 110000011 101110111 001001111
	100	000110011 001011010 100001101 111111110
	101	110101011 000110101 011101011 100101011
	110	001001101 101111111 011010001 001110100
	111	011010111 010101111 000111110 010010011

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_ViterbiBitDCC



Description Viterbi decoder bit by bit for convolutional code
Library EDGE, Channel Coding
Class SDFEDGE_ViterbiBitDCC
Derived From EDGE_ViterbiDecoder

Parameters

Name	Description	Default	Sym	Type	Range
CodeRate	convolutional code rate.	2	N	int	†
ConstraintLength	convolutional code constraint length.	9	K	int	(1, 9]
Polynomials	convolutional code polynomials, in terms of octal number	0753 0561		int array	††

† CodeRate ≥ 1. Reciprocals are used to represent fractional code rates: 1 = code rate 1; 2 = code rate 1/2; 3 = code rate 1/3.† † Octal numbers are used to indicate generator polynomials; one digit in an octal number corresponds to 3 digits in a binary number; the bit number of each polynomial can be evenly divided by 3. If the constraint length (assumed to be K) cannot be evenly divided by 3, only higher K generator bits are used; other (lower) bits are all 0s. The MSB represents the term without delay in the polynomial; delay increases left to right. For example, the generator g0 is $1+D^3+D^4+D^5+D^6$, which has a constraint length of 7; the polynomials are written as 100111100 (that is, 0474).

Pin Inputs

Pin	Name	Description	Signal Type
1	input	code words to be viterbi-decoded.	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	decoded bits.	int

Notes/Equations

This model is used to Viterbi-decode the input code words. There is a delay the length of which equals to the memory length of convolutional code due to the constraint length of convolutional code. The length of delay is 5 × K. Padding bits are used in order for the model to detect when the code words end.

One output token is produced when CodeRate input tokens are consumed.

References

1. S. Lin and D. J. Costello, Jr., *Error Control Coding Fundamentals and Applications* , Prentice Hall, Englewood Cliffs NJ, 1983.
2. Raymond Steele, Mobile Radio Communication, London: Pentech Press, 1992.

EDGE Base Station Receiver Design Examples

Introduction

The BTS_RX_wrk workspace provides design examples of base station receiver measurements including static reference sensitivity levels, multipath reference sensitivity levels, reference interference levels, and blocking characteristics. Measurements are based on GSM 11.21 Chapter 7 and corresponding EDGE *Change Request* documents.

Design examples include:

- Static reference sensitivity level measurements: BTS_RxSRSL_MCS5, BTS_RxSRSL_MCS6, BTS_RxSRSL_MCS7, BTS_RxSRSL_MCS8 and BTS_RxSRSL_MCS9.
- Multipath reference sensitivity level measurements: BTS_RxMRSL_MCS5, BTS_RxMRSL_MCS6, BTS_RxMRSL_MCS7, BTS_RxMRSL_MCS8 and BTS_RxMRSL_MCS9.
- Reference interference level measurements: BTS_RxRIL_CoCH, BTS_RxRIL_1stAdCH and BTS_RxRIL_2ndAdCH.
- Blocking characteristics: BTS_RxPreBlocking and BTS_RxBlocking_Test.

Designs in this workspace include:

- MS signal source in baseband
  EDGE_MS_MCSN_PwrCtrlSrc (N = 5, ... , 9) generates the encoded, framed and modulated uplink baseband signal for EDGE. The power level of each time slot of the signal can also be controlled with this source.
- Transmission modulation and up-converter
  Data from EDGE_MS_MCSN_PwrCtrlSrc is up-converted to 71 MHz IF signal with EDGE_RF_Mod, then modulated into an 890 MHz RF signal with EDGE_RF_TX_IFin.
- Channel loss and interfering signal combination
  The transmitted RF signal is then attenuated by RF channel (GainRF model) and combined with interfering signals (modulated or continuous waveform) at specified frequency offsets. Propagation conditions are also simulated in some designs.
- Down-converter and demodulation
  At the receiver side, the received signal is demodulated to be the baseband signal by EDGE_RF_RX_IFout and EDGE_RF_Demod.
- Base station receiver in baseband
  EDGE_BTS_MCSN_Receiver (N = 5, ..., 9) is used to demodulate and decode the received baseband signals.

Static Reference Sensitivity Level Measurements

BTS_RxSRSL_MCS5
BTS_RxSRSL_MCS6
BTS_RxSRSL_MCS7
BTS_RxSRSL_MCS8
BTS_RxSRSL_MCS9

Features

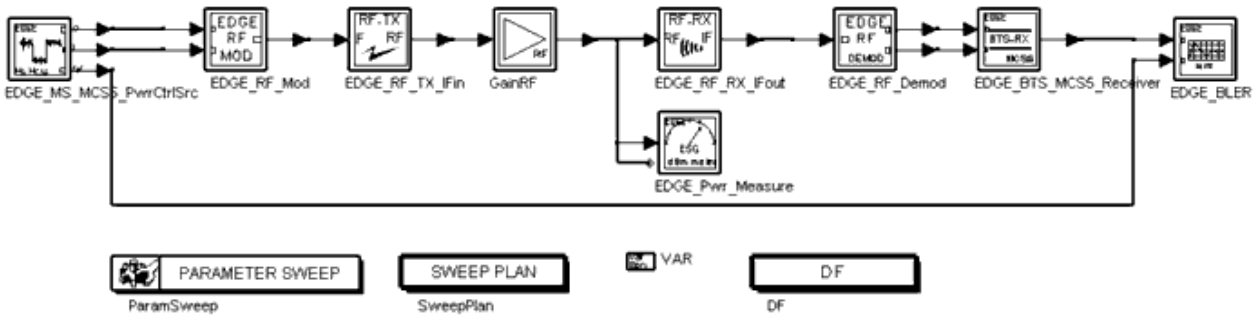
- minimum input performance levels under static conditions
- swept ARFCN 1, 63, 124
- BLER and BER measurements

Description

These designs measure the static reference sensitivity level of base station receiver using coding schemes MCS5 to MCS9.

The static reference sensitivity level is the signal level at the receiver input with a standard test signal. Using this test signal, the receiver will produce data with a block error ratio that is better than or equal to that for a specific logical channel under static propagation conditions.

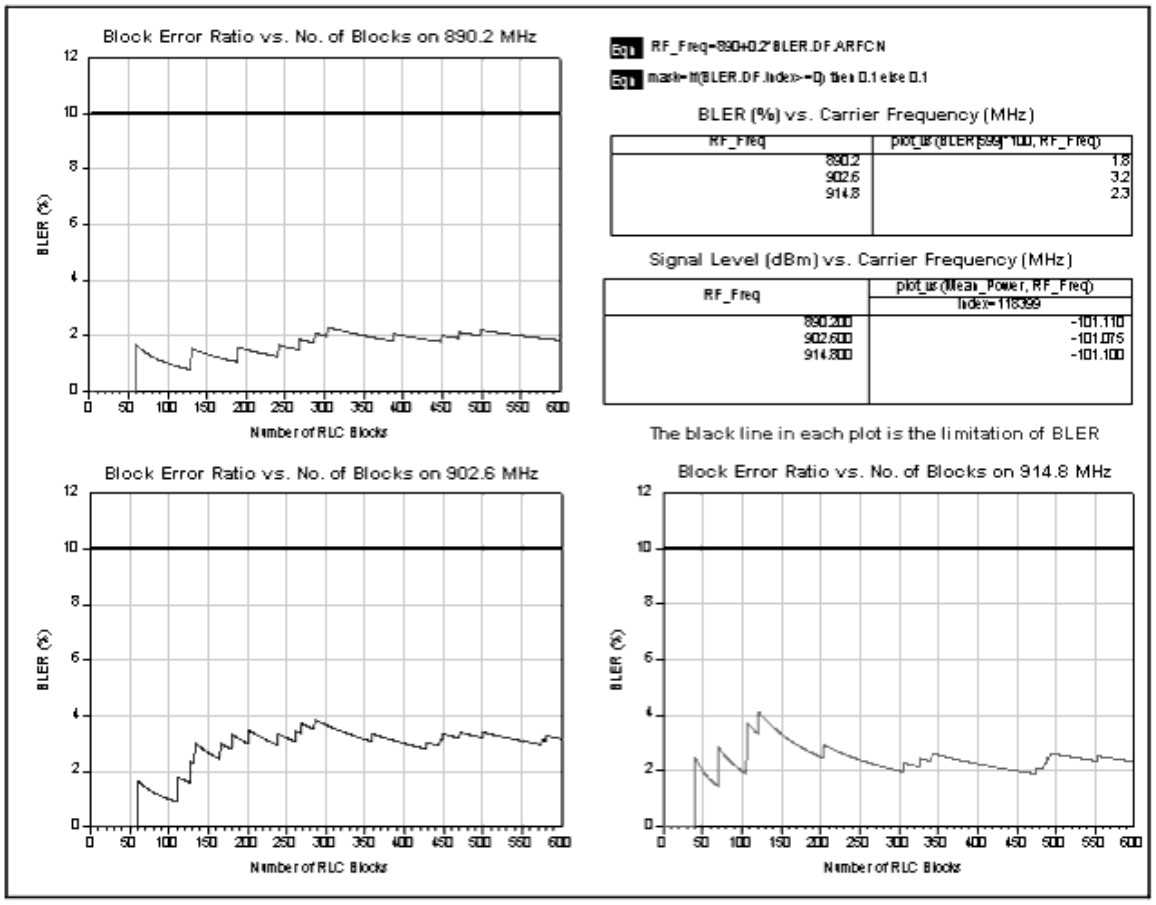
Schematic



BTS_RxSRSL_MCS5 Schematic

Test Results

Test results for MCS5 coding displayed in the BTS_RxSRSL_MCS5.dds file are shown in the following figure.



BTS_RxSRSL_MCS5.dds;

BLER for different ARFCN

Benchmark

- Hardware platform: Pentium III 800 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Data points: 600×3 blocks
- Simulation time: approximately 19.4 hours

Multipath Reference Sensitivity Level Measurements

BTS_RxMRSL_MCS5
BTS_RxMRSL_MCS6
BTS_RxMRSL_MCS7
BTS_RxMRSL_MCS8
BTS_RxMRSL_MCS9

Features

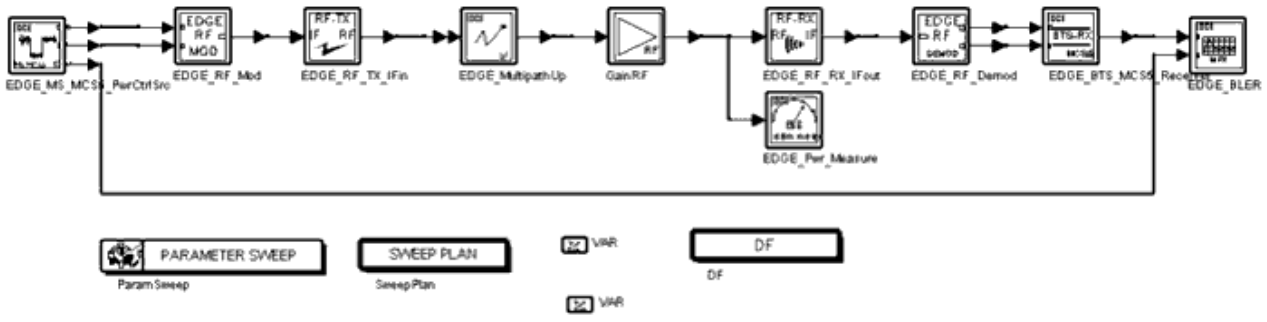
- minimum input performance levels under multipath conditions
- swept ARFCN 1, 63, 124
- BLER and BER measurements

Description

These designs measure the multipath reference sensitivity level of base station receiver using coding scheme MCS5 to MCS9.

The multipath reference sensitivity level of the receiver is the signal level at the receiver input with a standard test signal the receiver will produce after demodulation and channel decoding data with a block error ratio equal to or better than that for a specific logical channel under multipath propagation conditions.

Schematic



BTS_RxMRSL_MCS5 Schematic

Co-Channel Reference Interference Level Measurements

BTS_RxRIL_CoCH

Features

- integrated RF section
- GMSK modulated continuous interference signal
- C/Ic measured and calibrated
- propagation model

Description

This design measures the BTS receiver co-channel reference interference level. The test is based on specifications and requirements of GSM 11.21 Section 7.5 and corresponding EDGE *Change Request* documents.

The co-channel reference interference level is a measure of the receiver's ability to receive the desired modulated signal without exceeding a given degradation due to the presence of an unwanted modulated signal, both signals being at the nominal receiver frequency. The desired signal in this test is the signal generated by the transmitted RLC data blocks.

In this test, the mobile station transmits packets on PDTCH using MCS5 coding to the BTS on the allocated time slot (TS_Measured). The same power level is used on all other time slots. The co-channel interference ratio is set according to the following table.

MCS5 is tested in this example. Tests for MCS5 to MCS9 can be implemented using models EDGE_MS_MCSN_PwrCtrlSrc and EDGE_BTS_MCSN_Receiver, where N = 5, ... , 9).

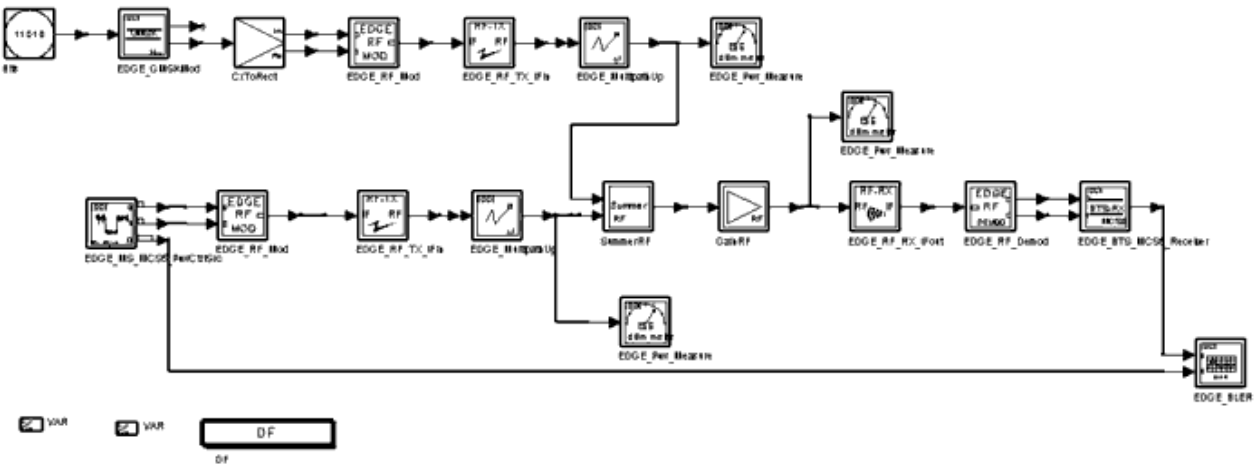
Test requirement: block error rate performance for MCS5, ... , MCS9 not to exceed 10% or 30% depending on coding schemes at co-channel interference ratios (C/Ic) as listed in the following table.

Co-Channel Interference Ratios (C/Ic) for Packet Switched Channels and ECSD

GSM 400, GSM 900, GSM 850, and MXM 850					
Type of Channel	**Propagation Conditions**				
	TU3 (no SFH)	**TU50(no SFH)**	**TU50(ideal SFH)**	**RA250(no SFH)**	**TI5 (no SFH)**
PDTCH MCS-5 (dB)	18	15.5	14.5	16	19.5
PDTCH MCS-6 (dB)	20	18	17.5	21	22
PDTCH MCS-7 (dB)	23.5	24	24.5	26.5 †	28
PDTCH MCS-8 (dB)	28.5	30	30	† †	34
PDTCH MCS-9 (dB)	30	33	35	† †	37
† Performance is specified at 30% BLER. † † Cannot meet the reference performance.					

Schematic

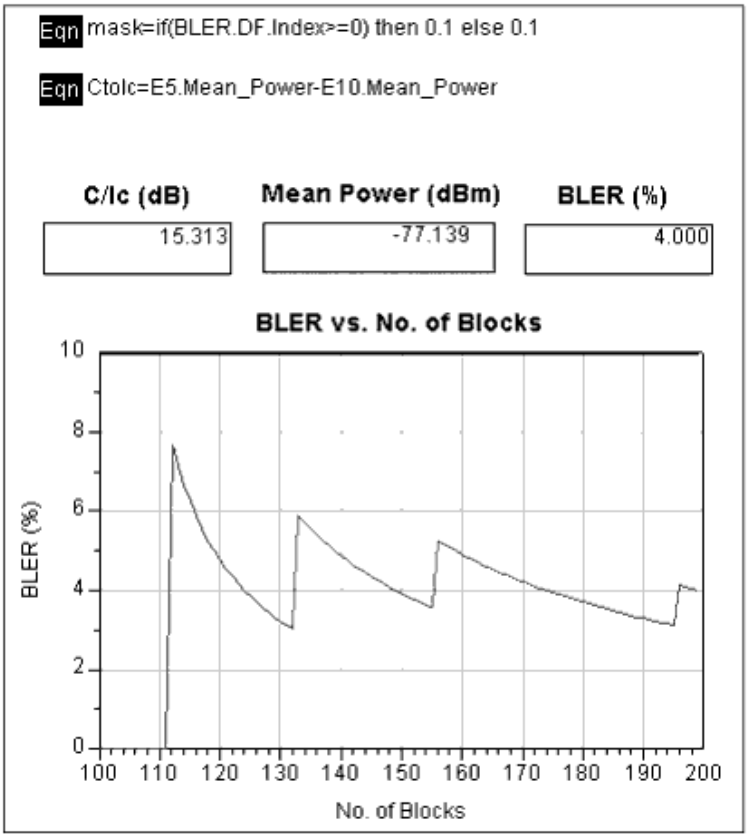
The schematic for this design is shown in the following figure. EDGE_MS_MCS5_PwrCtrlSrc generates the PDTCH MCS5 packages and outputs the original source data as the reference for BLER calculation. Power for each time slot of the TDMA frame is controlled by this source. The branch in the upper portion of the schematic generates the GMSK modulated interference signal. EDGE_Pwr_Measure subnetworks are used to measure power for the calibration of the C/Ic. EDGE_BTS_MCS5_Receiver retrieves the original source data using RSSE (reduced-state sequence estimation) and the MCS5 decoder. Data at the output of the receiver is then used for BLER calculation.



BTS_RxRIL_CoCH Schematic

Test Results

Test results displayed in the BTS_RxRIL_CoCH.dds file are shown in the following figure. Results meet the test requirements.



BTS_RxRIL_CoCH.dds

Benchmark

- Hardware platform: Pentium III 800 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 100 RLC blocks
- Simulation time: approximately 11.6 hours

Adjacent Channel Reference Interference Level Measurements

BTS_RxRIL_1stAdCH
BTS_RxRIL_2ndAdCH

Features

- measurement of base station receiver adjacent channel selectivity
- integrated RF models
- BLER of PDTCH
- mean power of desired signal through a TU50 fading channel
- mean power of adjacent channel interferer through a TU50 channel

Description

These designs measure base station receiver adjacent channel sensitivity according to GSM 11.21 section 7.5 and corresponding EDGE *Change Request* documents. MCS5 is tested as an example.

BTS_RxRIL_1stAdCH is for the first adjacent channel interference test, and BTS_RxRIL_2ndAdCH is for the second adjacent channel interference test.

The adjacent channel selectivity is a measure of the capability of the receiver to receive the wanted data packets without exceeding a given degradation due to the presence of an interfering signal (I1) in the adjacent channel. Wanted signal in this test is the signal generated by the transmitted RLC data blocks.

The adjacent channel can be adjacent in the RF spectrum or in time. In this test, adjacent RF channel selectivity test is performed.

For packet switched channels, the desired signal level is (X −9 dB + C/Ic), where X is the power level defined in the first of the following four tables; C/Ic is the co-channel interference ratio defined in the second table; the interfering signal level will be determined by C/Ia, where C/Ia is the adjacent channel interference ratio defined in the third table. BLER performance must be less than the error performance limits defined in the fourth table.

Test Signal Average Input Level for Reference Interference Level Measurements

BTS Type	Test Signal Average Input Level to Receiver
GSM 400/GSM900/DCS1800/PCS 1900/GSM 850/ MXM 850/MXM 1900 BTS	-84 dBm
GSM900/GSM 850/MXM 850 micro-BTS M1	-77 dBm
GSM900/GSM 850/MXM 850 micro-BTS M2	-72 dBm
GSM900/GSM 850/MXM 850 micro-BTS M3	-67 dBm
GSM900/GSM 850/MXM 850 pico-BTS P1	-68 dBm †
DCS1800/PCS 1900/ MXM 1900 micro-BTS M1	-82 dBm
DCS1800/PCS 1900/ MXM 1900 micro-BTS M2	-77 dBm
DCS1800/PCS 1900/ MXM 1900 micro-BTS M3	-72 dBm
DCS1800/PCS 1900/ MXM 1900 pico-BTS P1	-75 dBm †
† The power level should be 4 dB greater for measurements performed with interferer offsets of 400 kHz or greater.	

Co-channel and Adjacent Channel Interference Ratios for GPRS, EGPRS and ECSD channel

Interferer Offset	Carrier to Interferer Ratio GMSK	Carrier to Interferer Ratio 8PSK	Interferer Fading
0 kHz	C/Ic (Co-Channel Interference Ratios (C/Ic) for Packet Switched Channels and ECSD)	C/Ic (Co-Channel Interference Ratios (C/Ic) for Packet Switched Channels and ECSD)	yes
200 kHz	C/Ic - 18 dB	(Adjacent Channel Interference Ratios (C/Ia) for EGPRS Channels)	yes
400 kHz	C/Ic - 50 dB	C/Ic - 50 dB	no

Adjacent Channel Interference Ratios (C/Ia) for EGPRS Channels

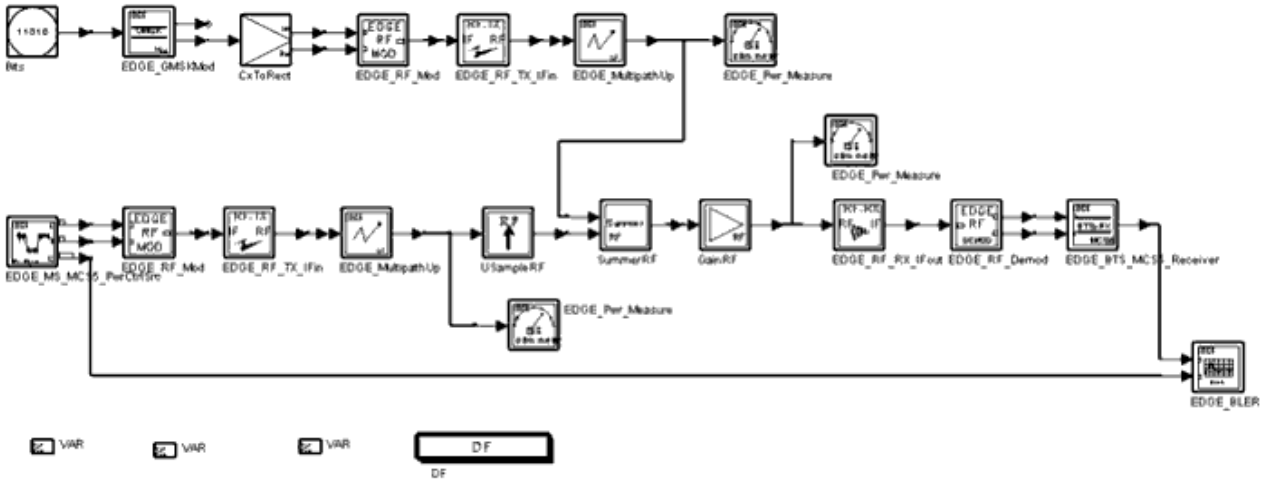
GSM 400, GSM900, GSM 850 and MXM 850					
Channel Type	**TU3 (no SFH)**	**TU50 (no SFH)**	**TU50 (ideal SFH)**	**RA250 (no SFH)**	**T15 (no SFH)**
PDTCH/MCS-5	2.5 dB	2 dB	2 dB	1 dB	(tbd)
PDTCH/MCS-6	4.5 dB	1 dB	1 dB	6.5 dB	(tbd)
PDTCH/MCS-7	8 dB	8.5 dB	8.5 dB	13.5 dB †	(tbd)
PDTCH/MCS-8	10.5 dB	9 dB †	9.5 dB †	††	(tbd)
PDTCH/MCS-9	12 dB	13.5 dB †	13.5 dB †	††	(tbd)
† Performance is specified at 30% BLER. †† Tests not performed.					

GSM 400, GSM900, GSM 850 and MXM 850 Multipath Error Performance Limits at RX Interference Level

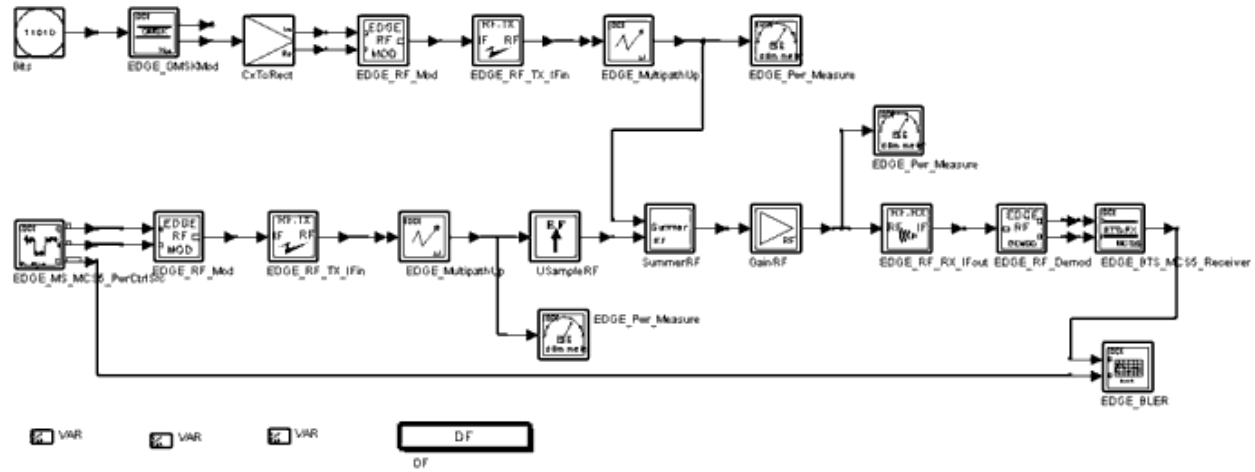
Channel Type	Error Measure	Error Ratios for Specified Propagation Conditions				
		TU3(no SFH)	TU50(no SFH)	TU50(ideal SFH)	RA250(no SFH)	TI5(no SFH)
PDTCH/MCS-1 to 6	(BLER)	10%	10%	10%	10%	10%
PDTCH/MCS-7	(BLER)	10%	10%	10%	30%	10%
PDTCH/MCS-8	(BLER)	10%	30%	30%	†	30%
PDTCH/MCS-9	(BLER)	10%	30%	30%	†	30%

† Tests not performed.

Schematic



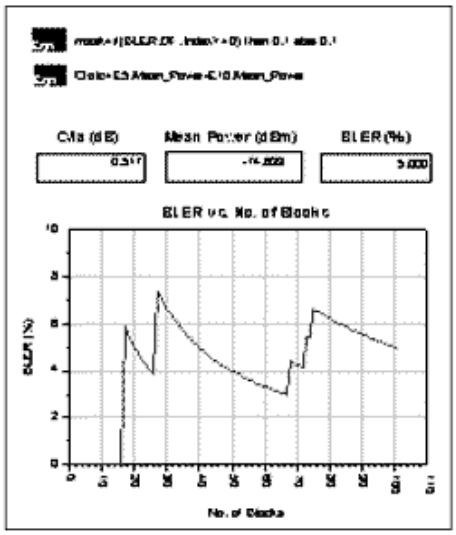
BTS_RxRIL_1stAdCH Schematic



BTS_RxRIL_2ndAdCH Schematic

Test Results

The test is performed only for PDTCH/MCS5, TU50, the first adjacent channel. Test results displayed in BTS_RxRIL_1stAdCH.dds are shown in the following figure. Results meet the requirements.



BTS_RxRIL_1stAdCH.dds

Benchmark

- Hardware platform: Pentium III 800 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Data points: 100 blocks
- Simulation time: 5 hours 3 minutes

Blocking Characteristics Measurements

BTS_RxPreBlocking
BTS_RxBlocking_Test

Features

- base station receiver blocking characteristics
- RF models integrated
- BLER (block error rate) of PDTCH
- mean power of desired signal at the receiver input
- mean power of interferer at the receiver input

Description

These designs test the blocking characteristics according to GSM 11.21 Section 7.6 and corresponding EDGE *Change Request* documents. MCS5 is used in this test.

Blocking is a measure of the BSS receiver's ability to receive the desired GSM modulated signal in the presence of an interfering signal.
BTS_RxPreBlocking is for an optional preliminary test to reduce the number of measurements required in the blocking characteristics test. This design demonstrates how to carry out the preliminary test; only two frequency points are swept.

BTS_RxBlocking_Test is for the blocking characteristics test. This test assumes the preliminary test failed at two frequencies that are 600 kHz apart from the frequency of the desired signal.

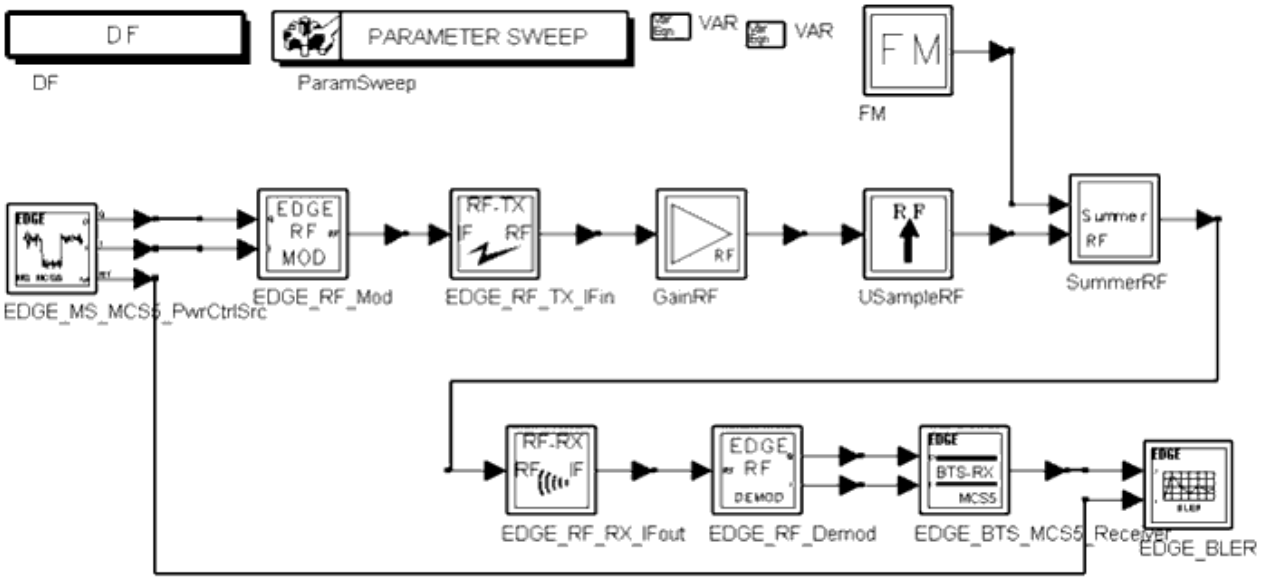
The power level of desired signal PDTCH/MCS-5 is -98 dBm, and the power level of interfering signal is shown in the following table.

The BLER must be below the 10% limit.

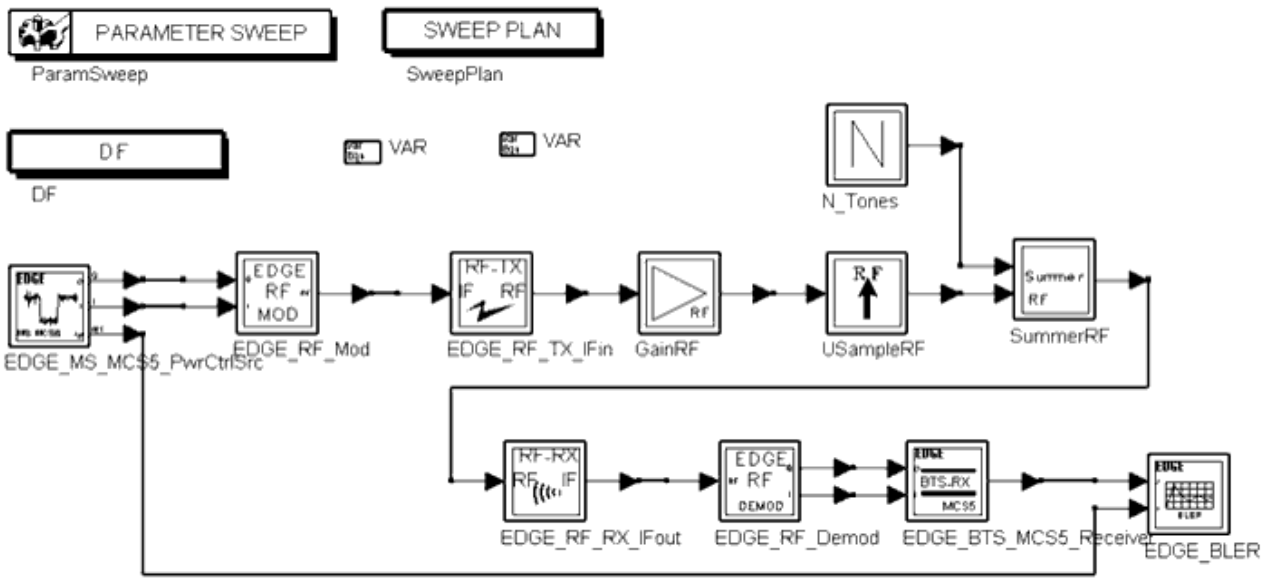
Level of Interfering Signal for Blocking

GSM 400 and GSM900 (dBm)	**BTS**	**micro and pico-BTS**			
		M1	**M2**	**M3**	**P1**
inband					
+/- 600 kHz	-26	-31	-26	-21	-34
800 kHz ≤ |f-fo| < 1.6 MHz	-16	-21	-16	-11	-34
1.6 MHz ≤ |f-fo| < 3 MHz	-16	-21	-16	-11	-26
3 MHz ≤ |f-fo|	-13	-21	-16	-11	-18
out-of-band	8	8	8	8	8

Schematic



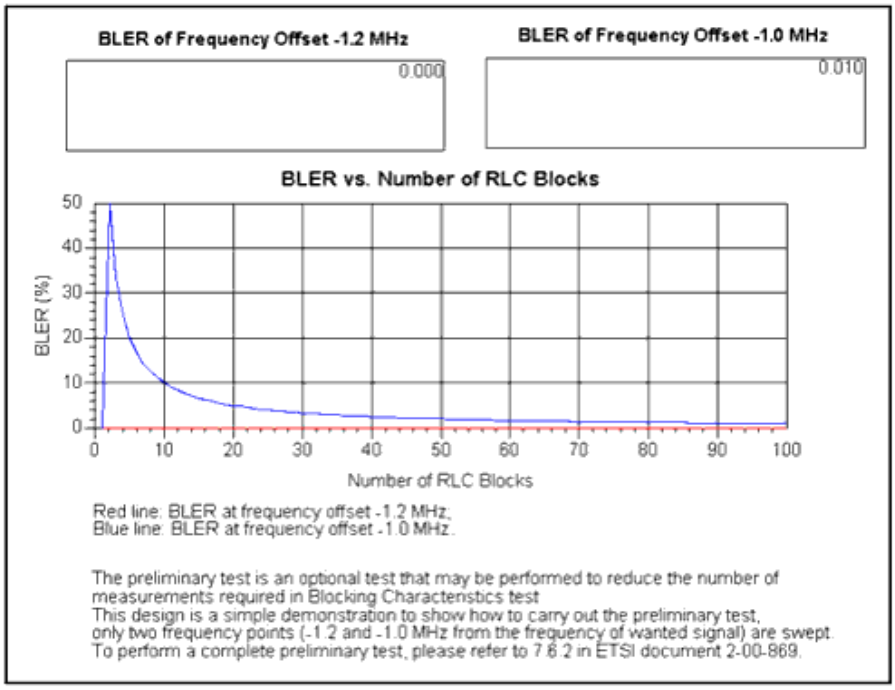
BTS_RxPreBlocking Schematic



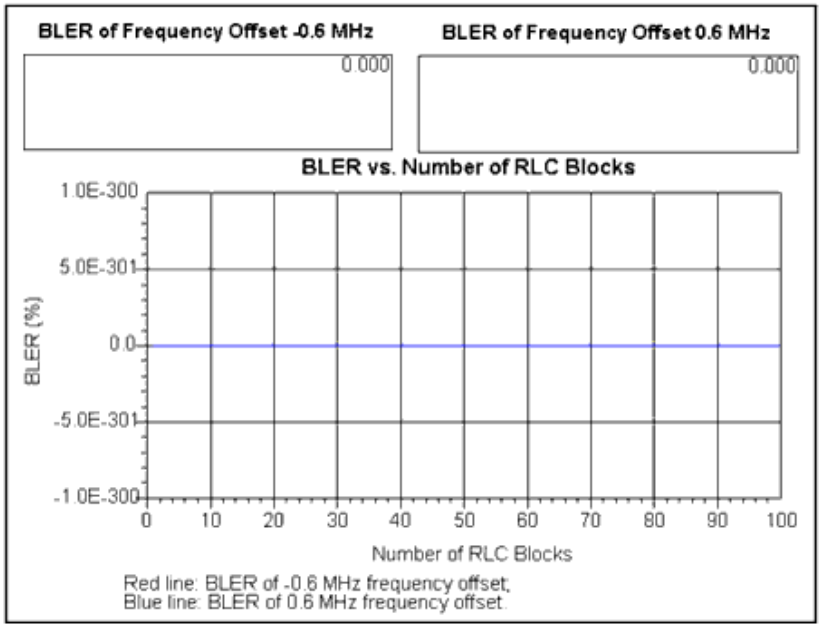
BTS_RxBlocking_Test Schematic

Test Results

Test results displayed in BTS_RxPreBlocking.dds and BTS_RxBlocking_Test.dds are shown in the following two figures. Tests results meet the requirements.



BTS_RxPreBlocking.dds



BTS_RxBlocking_Test.dds

Benchmark for BTS_RxPreBlocking

- Hardware platform: Pentium III 500 MHz, 128 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3

- Data points: 100 blocks
- Simulation time: approximately 6.5 hours

Benchmark for BTS_RxBlocking

- Hardware platform: Pentium III 500 MHz, 128 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Data points: 100 blocks
- Simulation time: approximately 5 hours

EDGE Base Station Transmitter Design Examples

Introduction

The BTS_TX_wrk workspace provides design examples of base station transmitter measurements including modulation accuracy, mean transmitted RF carrier power, transmitted RF carrier power versus time, and adjacent channel power. Measurements are based on chapter 6 of GSM 11.21 and corresponding EDGE *Change Request* documents.

Designs for these measurements include:

- Modulation accuracy: BTS_TxEVM_2pin and BTS_TxEVM_1pin
- Mean transmitted RF carrier power: BTS_TxMeanPwr
- Transmitted RF carrier power versus time: BTS_TxPwr_vs_Time
- Adjacent channel power: BTS_TxORFS_Modulation and BTS_TxORFS_Switching
- Switching transients spectrum
  Designs in this workspace consist of:
- User equipment signal source in baseband
  - EDGE_ActiveIdleSrc provides framed and modulated baseband signal for EDGE.
  - EDGE_RandomSrc provides continuous, random and modulated baseband signal for EDGE.
- Transmit modulation and up-converter
  Data from the baseband signal source for EDGE is up-converted to 71 MHz with EDGE_RF_Mod, then modulated into a 935 MHz RF signal with EDGE_RF_TX_IFin.

Modulation Accuracy EVM Measurements

BTS_TxEVM_2pin
BTS_TxEVM_1pin

Features

- 2- and 1-pin EVM models
- RMS, peak, and 95th percentile EVM measurements
- 8PSK modulation with pulse-shaping filter and continuous $\frac{3}{8}\pi$ symbol phase rotation
- adjustable sample rate
- integrated RF section
- circuit envelope co-simulation for RF transmitter
- EDGE measurement filter (raised-cosine-windowed-raised-cosine filter)

Description

These designs demonstrate 8PSK modulation accuracy of BTS by measuring the EVM. Test in these designs are implemented according to the methods and requirements described in 6.2 of GSM 11.21 and the corresponding *Change Request*.
Test requirements are:

- RMS EVM not to exceed 7.0%
- (averaged) peak EVM not to exceed 22%
- 95th percentile EVM not to exceed 11%
  For EVM calculation the transmitted signal is modeled by:

  $Y(t) = C1\{R(t) + D(t) + C0\}W^t$
  R(t) is defined to be an ideal transmitter signal (reference signal)
  D(t) is the residual complex error on signal R(t)
  C0 is a constant origin offset representing carrier feed-through
  C1 is a complex constant representing the arbitrary phase and output power of the transmitter
  $W = e^{\alpha + j2\pi f}$
  accounts for both a frequency offset of 2πf radians per second phase rotation and an amplitude change of α nepers per second

  The symbol timing phase of Y(t) is aligned with R(t).
  The transmitted signal Y(t) is compensated in amplitude, frequency and phase by multiplying with the factor:

  $W^{-t}/C1$

  The values for W and C1 are determined using an iterative procedure. W(α,f), C1 and C0 are chosen to minimize the RMS value of EVM.
  After compensation, Y(t) is passed through the specified measurement filter (GSM 05.05, 4.6.2) to produce the signal

$$Z(k) = S(k) + E(k) + C0$$

where

S(k) is the ideal transmitter signal observed through the measurement filter

k = floor (t/T_s), where T_s =1/270.833 kHz corresponding to the symbol times

The error vector is defined to be:

$$E(k) = Z(k) - C0 - S(k)$$

It is measured and calculated for each instant k over the useful part of the burst excluding tail bits. The RMS vector error is defined as:

$$\text{RMS EVM} = \sum_{k \in K} |E(k)|^2 / \sum_{k \in K} |S(k)|^2$$

The peak EVM is the peak error deviation within a burst, measured at each symbol interval, averaged over at least 200 bursts.

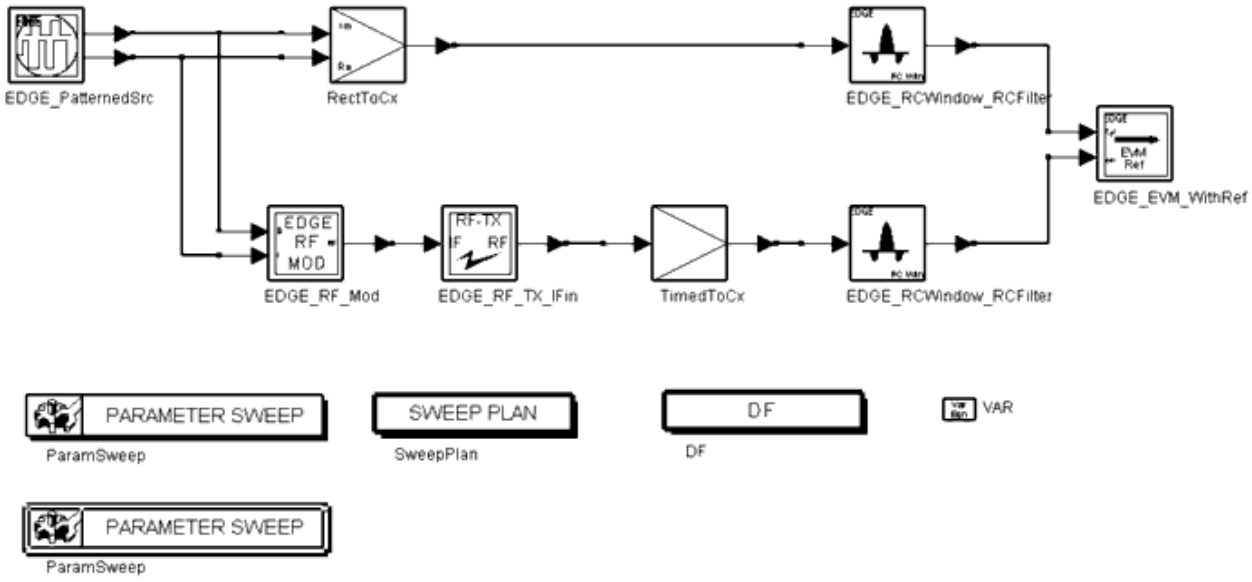
The 95th percentile EVM is the point where 95% of the individual EVM (measured at each symbol interval) is below that point. That is, only 5% of the symbols are allowed to have an EVM exceeding the 95th-percentile point. EVM values are acquired during the useful part of the burst, excluding tail bits, over 200 bursts.

Schematics

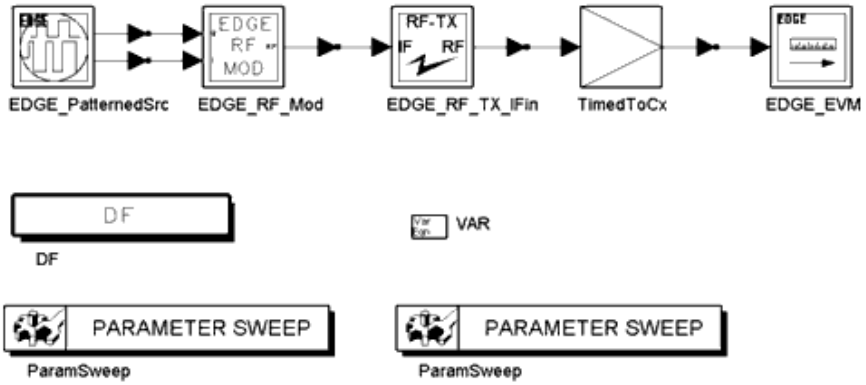
The BTS_TxEVM_2pin schematic is shown in the first of the following two figures. EDGE_RandomSrc is a continuous random source generating 8PSK modulated signals. The upper path is for reference signal, which is an ideal transmitter signal that provides prior information for the EVM model. The raised-cosine-windowed raised cosine filters used before EDGE_EVM_WithRef is the EDGE measurement filter.

The BTS_TxEVM_1pin schematic is shown in the second of the following two figures. In this design, the original transmitted signal is retrieved inside the 1-pin EVM subnetwork after demodulation, so the reference signal is no longer needed.

In both designs NumBursts is set to 200 to obtain the averaged results over 200 bursts; SymBurstLen is set to 142, which is derived from the equation:
142(length of useful part) =
156 (length of whole burst) −8 (guard symbols) −6 (tail symbols)



BTS_TxEVM_2pin Schematic



BTS_TxEVM_1pin Schematic

Test Results

EVM Results of 2-pin EVM

	ARFCN 1 (%)	ARFCN 63 (%)	ARFCN 124 (%)
RMS EVM	5.260	5.138	5.265
Peak EVM	10.511	10.151	10.588
95:th percntile EVM	8.791	8.510	8.751

EVM Results of 1-pin EVM

	ARFCN 1 (%)	ARFCN 63 (%)	ARFCN 124 (%)
RMS EVM	5.280	5.139	5.266
Peak EVM	10.478	10.187	10.549
95:th percntile EVM	8.782	8.513	8.749

Upper limit of the test requirement for RMS EVM is 8.0%.
Upper limit of the test requirement for peak EVM is 22.0%.
Upper limit of the test requirement for 95:th percentile EVM is 11.0%.

Benchmark

- Hardware Platform: Pentium III 800 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data Points: 9 × 200 bursts (9 × 142 × 200 = 255600 symbols)
- Simulation Time: approximately 110 minutes for BTS_TxEVM_1pin
  approximately 100 minutes for BTS_TxEVM_2pin

Mean Transmitted RF Carrier Power Measurements

BTS_TxMeanPwr

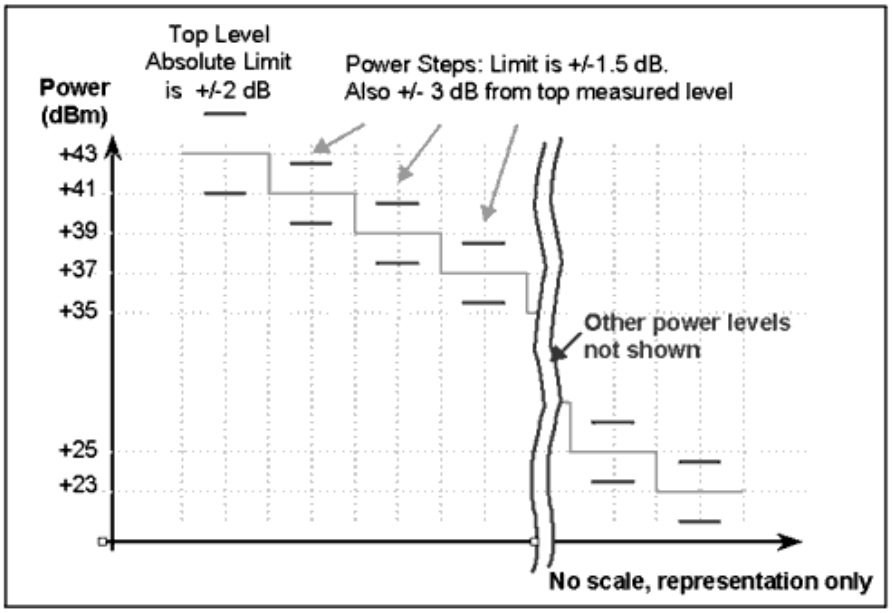
Features

- 8PSK modulation
- normal burst
- 11 power control levels from 23 to 43 dBm
- adjustable sample rate
- integrated RF section

Design Description

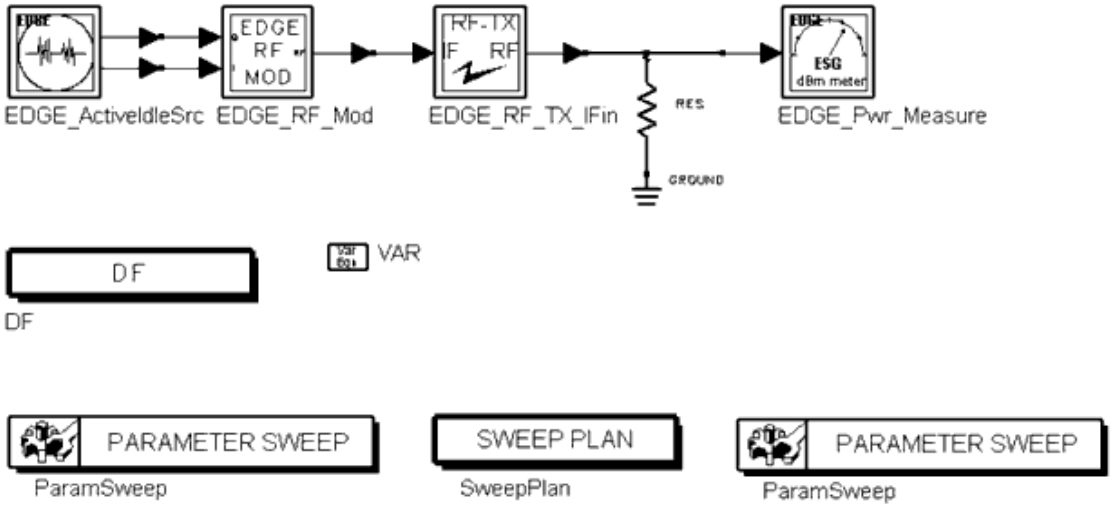
BTS_TxMeanPwr measures the mean transmitter output power of BTS to verify that all power control levels have output power within requirements.

Requirements for BTS output power vary according to manufacturer needs. The requirements of this test are illustrated in the following figure for normal conditions.



Transmitter Output Power for Various Power Control Levels with Tolerance

Schematic

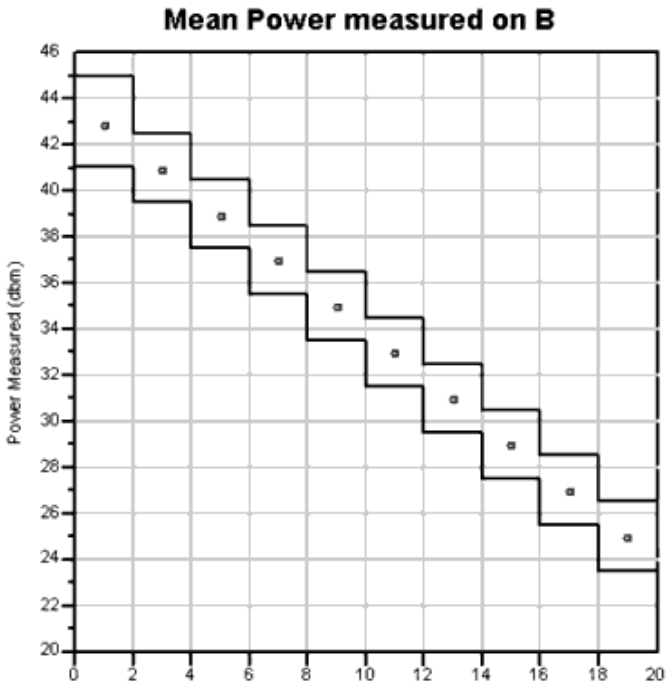


BTS_TxMeanPwr Schematic

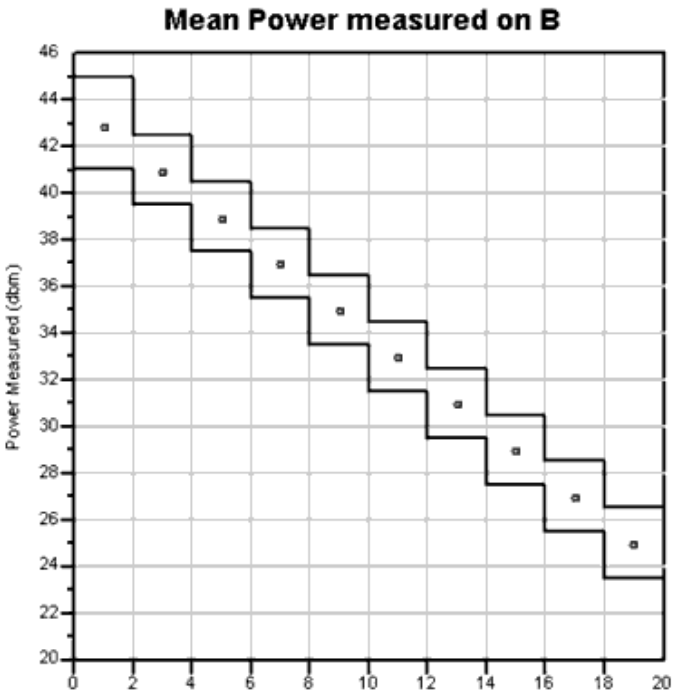
Test Results

The test results are shown in the following three figures for the lowest (935.2 MHz), middle (947.6 MHz), and highest (959.8 MHz) frequencies for which the test is performed. These figures are displayed in the BTS_TxMeanPwr.dds file in a data display window; blue lines represent the upper masks while black lines represent the lower masks; circular symbols represent the output mean power.

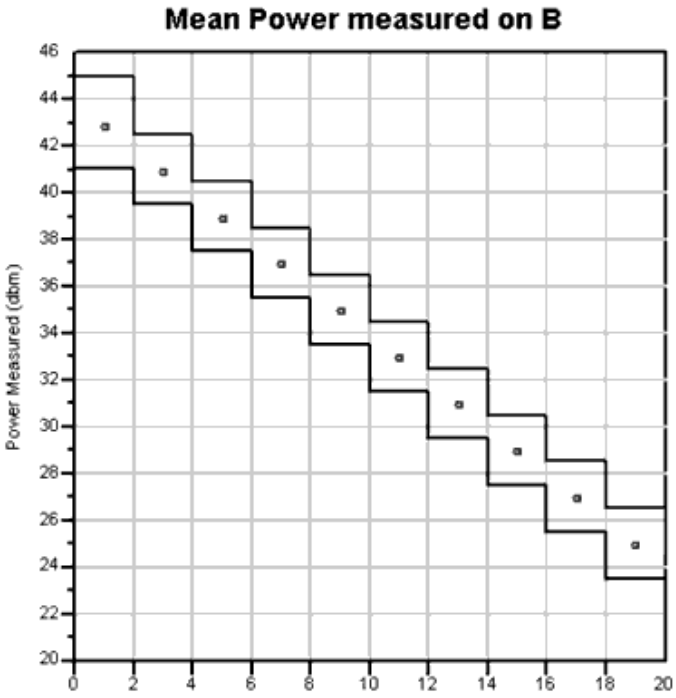
Transmitter output mean power of this design is within the requirements.



Mean Power, 935.2 MHz Frequency



Mean Power, 947.6 MHz Frequency



Mean Power, 959.8 MHz Frequency

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, ADS 1.3
- Time slots to be averaged: 200 time slots
- Simulation Time: approximately 20 hours

Transmitted RF Carrier Power versus Time Measurements

BTS_TxPwr_vs_Time

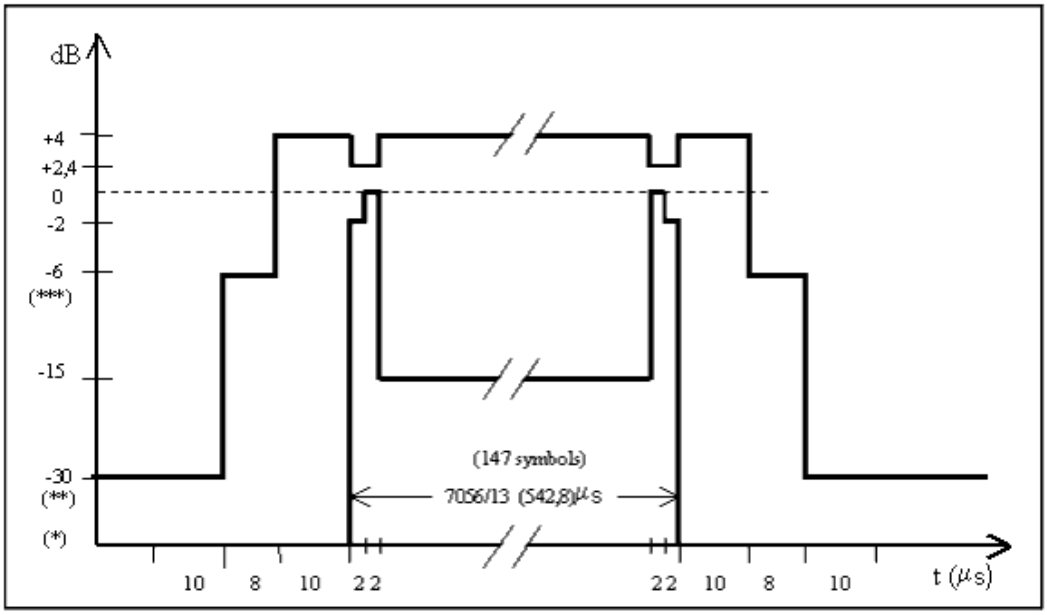
Features

- 8PSK modulation
- normal burst
- adjustable sample rate
- integrated RF section

Design Description

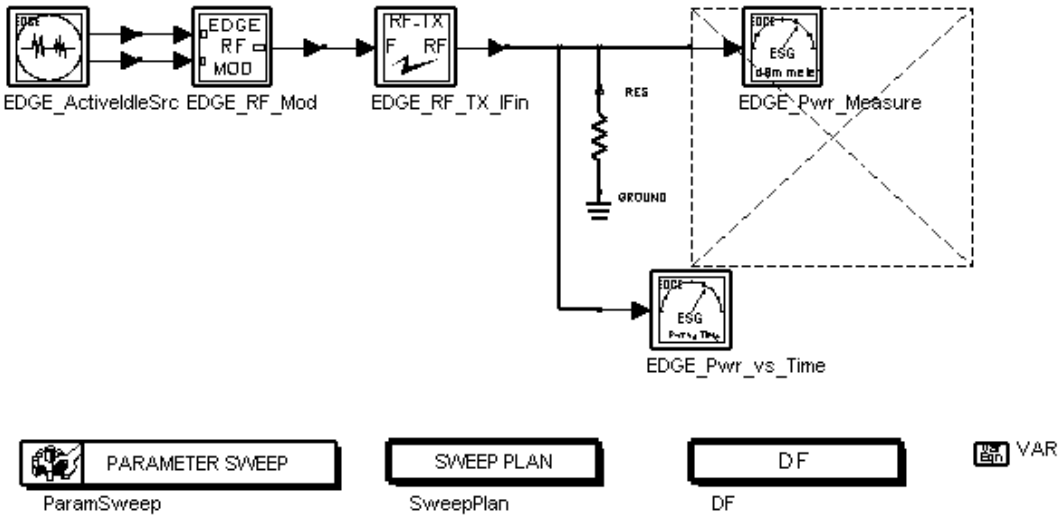
BTS_TxPwr_vs_Time measures the mobile station output power versus time to verify that the output power relative to time is within the requirements when sending a normal burst of the 8PSK modulated signals.

The transmitter power level relative to time for a normal burst must be within the power/time template illustrated in the following figure.



Time Mask for Normal Duration Bursts at 8PSK Modulation

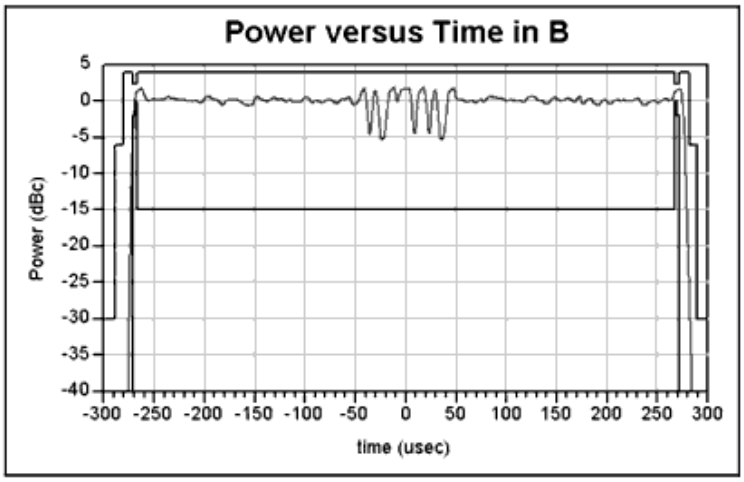
Schematic



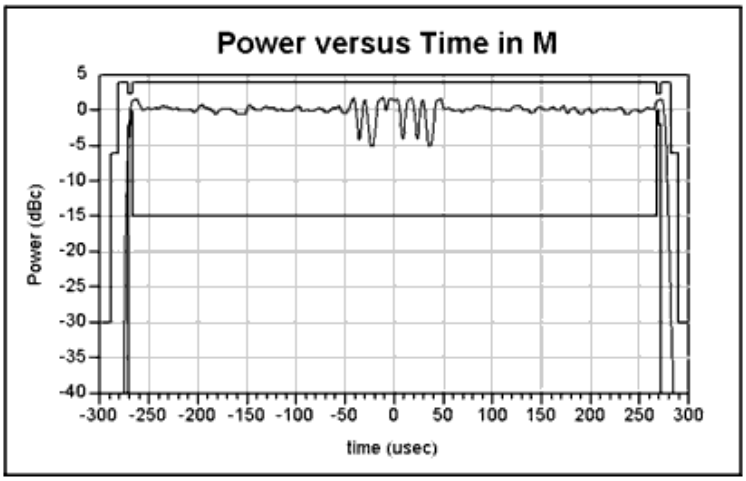
BTS_TxPwr_vs_Time Schematic

Test Results

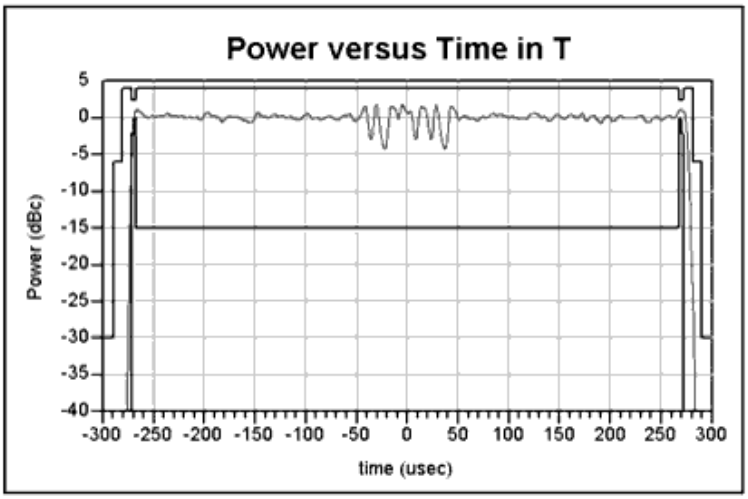
The test results are given in the following three figures for the lowest (935.2 MHz), middle (947.6 MHz), and highest (959.8 MHz) frequencies for which the test is performed. Transmitter output power versus time of this design is within the requirements.



Power versus Time, 935.2 MHz Frequency



Power versus Time, 947.6 MHz Frequency



Power versus Time, 959.8 MHz Frequency

Benchmark

- Hardware platform: Pentium II 400 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Time slots to be averaged: 200 time slots
- Simulation time: approximately 40 minutes

Adjacent Channel Power Measurements with Modulation and Wideband Noise

BTS_TxORFS_Modulation

Features

- 8PSK modulation with pulse-shaping filter and continuous $\frac{3}{8}\pi$ symbol phase rotation
- adjustable sample rate
- spectrum analysis and constellation display
- integrated RF section

Description

This example is used to verify that the output RF spectrum of the BTS due to modulation and wideband noise does not exceed the specified levels for an individual transceiver.3 Test requirements are:

- All time slots must be set up to transmit full power modulated with a pseudo-random bit sequence of encrypted bits.
- The power level must be measured for each power step to be tested.
- Using a filter and video bandwidth of 30 kHz, power must be measured at the antenna connector on the carrier frequency. The measurement must be gated over 50% to 90% of the useful part of the transmitted bursts excluding the midamble, and the measurement value over this part of the burst must be averaged.

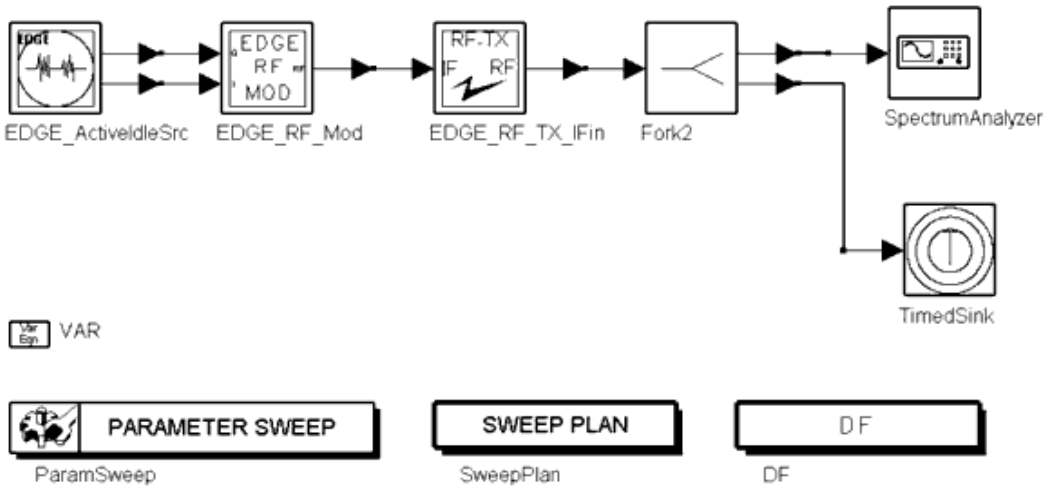
There are three test cases: low-, mid-, and high-range ARFCNs.

The output RF modulation spectrum is specified in the following table. The limits in the table, at the listed offsets from the carrier frequency, represent the ratio of measured power to the measured power for the same static power step. The table provides discrete power level requirements; for powers between those specified, linear interpolation must be applied.

Continuous Modulation Spectrum; Maximum Limits for BTS

Power Level (dBm) Step	Maximum Relative Level (dB) at Specified Carrier Offsets (kHz)							
	100	200	250	400	600 to <1200	1200 to <1800	1800 to <6000	>6000
	30 kHz Measurement (Filter) Bandwidth						100 kHz Measurement (Filter) Bandwidth	
≥43	+0.5	-30	-33	-60 †	-70	-73	-75	-80
41	+0.5	-30	-33	-60 †	-68	-71	-73	-80
39	+0.5	-30	-33	-60 †	-66	-69	-71	-80
37	+0.5	-30	-33	-60 †	-64	-67	-69	-80
35	+0.5	-30	-33	-60 †	-62	-65	-67	-80
≤33	+0.5	-30	-33	-60 †	-60	-63	-65	-80
† For equipment supporting 8PSK, the requirement at 8PSK modulation is -56 dB								

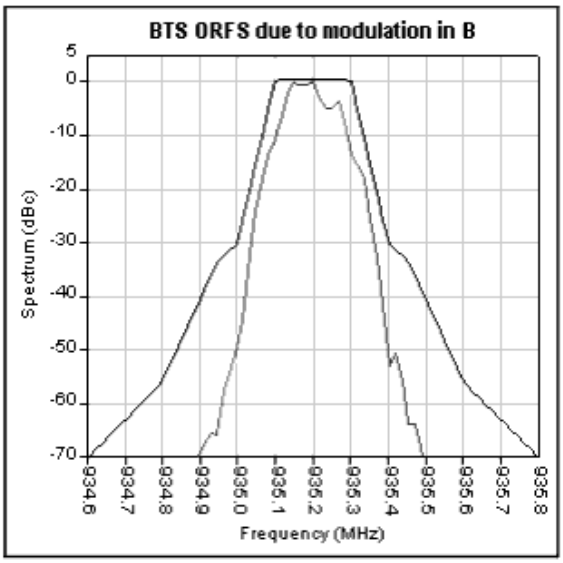
Schematic



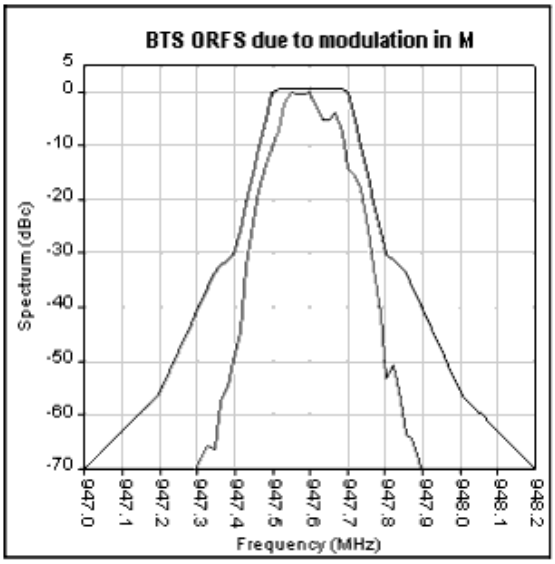
BTS_TxORFS_Modulation Schematic

Test Results

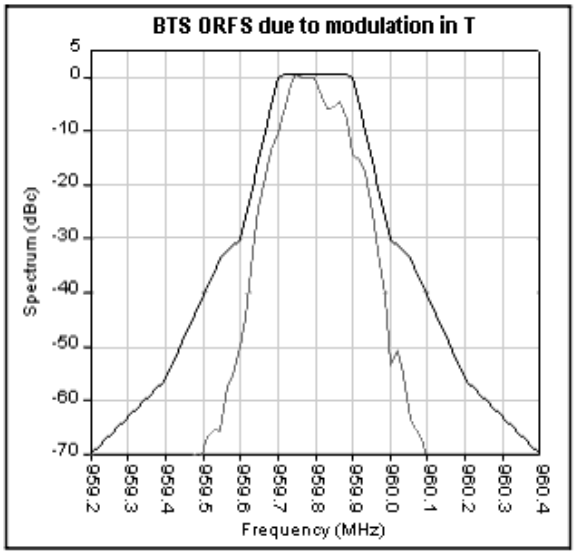
Test results are shown in the following three figures for the lowest (935.2 MHz), middle (947.6 MHz), and highest (959.8 MHz) frequencies for which the test is performed. The mask corresponds to power lever 43 in the preceding table.



BTS ORFS, 935.2 MHz Modulation



BTS ORFS, 947.6 MHz Modulation



BTS ORFS, 959.8 MHz Modulation

Benchmark

- Hardware platform: Pentium II 400 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Data points: 1 time slot
- Simulation time: 25 seconds

Adjacent Channel Power Measurements with Switching Transients

BTS_TxORFS_Switching

Features

- 8PSK modulation with pulse-shaping filter and continuous $\frac{3}{8}\pi$ symbol phase rotation
- adjustable sample rate
- spectrum analysis
- integrated RF section

Description

This example is used to show the spectrum of the signal from BTS due to switching transients, that is, the power ramping up and down. The output RF modulation spectrum maximum limits are specified in the following figure.

Test requirements are:

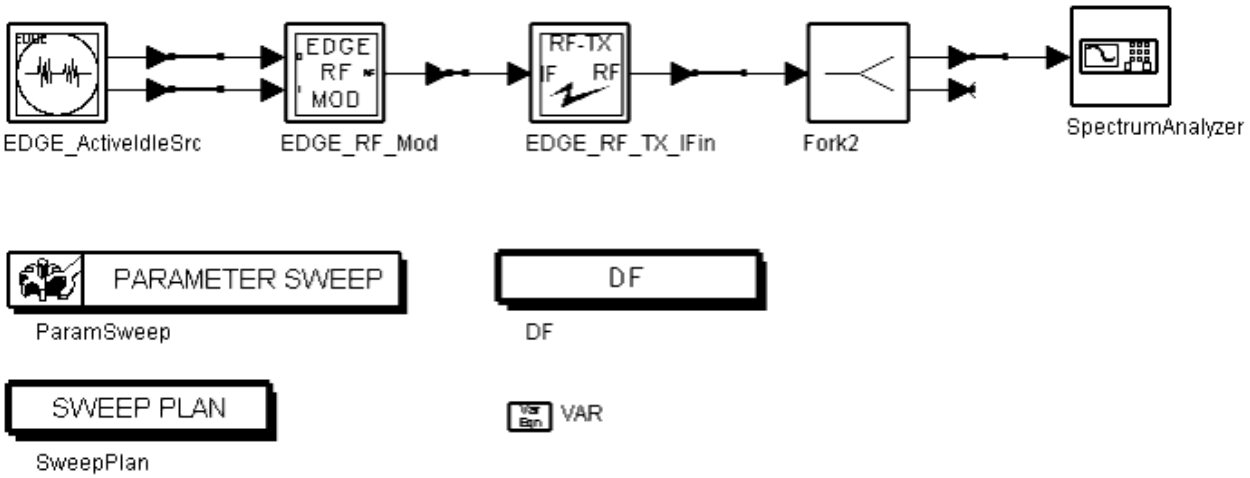
- zero frequency scan
- filter bandwidth of 30 kHz
- peak hold
- video bandwidth of 100 kHz

Switching Transients Spectrum - Maximum Limits

There are three test cases: low-, mid-, and high-range ARFCNs.

Offset (kHz)	Power (dBc): GSM 400, GSM900, GSM 850 and MXM 850 (GMSK)	Power (dBc): GSM 400, GSM900, GSM 850 and MXM 850 (8PSK)
400	-57	-52
600	-67	-62
1200	-74	-74
1800	-74	-74

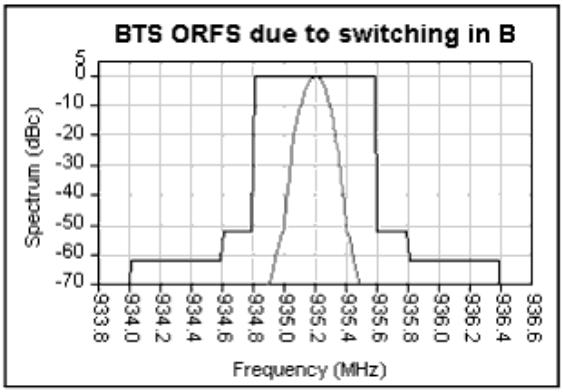
Schematic



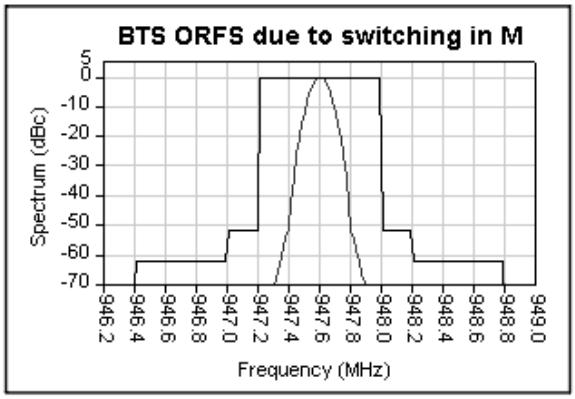
BTS_TxORFS_Switching Schematic

Test Results

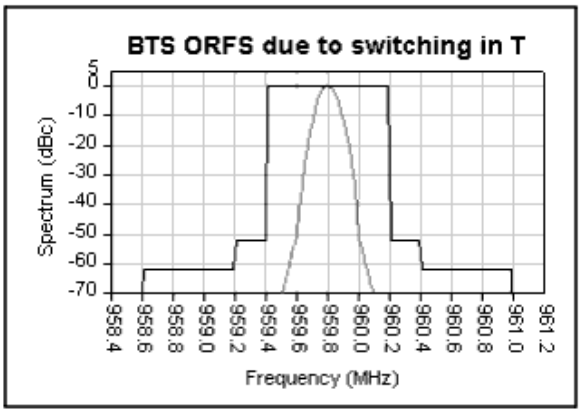
Test results are shown in the following three figures for the lowest (935.2 MHz), middle (947.6 MHz), and highest (959.8 MHz) frequencies for which the test is performed. The mask corresponds to power level 39 in the preceding table.



BTS ORFS, 935.2 MHz Switching



BTS ORFS, 947.6 MHz Switching



BTS ORFS, 959.8 MHz Switching

Benchmark

- Hardware platform: Pentium II 400 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Data points: 100 time slot
- Simulation time: 25 minutes

EDGE BER Validation Design Examples

Introduction

EDGE_BER_Validation Design Names

- MCS5_Static_AdaptiveEq
- MCS6_Static_AdaptiveEq
- MCS7_Static_AdaptiveEq
- MCS8_Static_AdaptiveEq
- MCS9_Static_AdaptiveEq
- Raw_Static_AdaptiveEq

Features

- End-to-end BER and BLER measurements in static propagation condition
- Adaptive equalizer
- Complete downlink
- Modulation and coding schemes MCS5 to MCS9
- Static AWGN propagation channel

Description

This workspace provides downlink end-to-end BER/BLER measurements under static propagation channel using ADS EDGE Design Library. MCS5 to MCS9 modulation and coding schemes for 8PSK are considered. A reduced-state sequence estimation (RSSE) adaptive equalizer is provided.

Designs using adaptive equalizers in the receiver provide BER/BLER measurements for modulation and coding schemes MCS5 through MCS9. A complete downlink is provided, including burst construction, 8PSK modulation, and synchronization.

The Raw_Static_AdaptiveEq provides BER measurement without channel coding. Adaptive equalizer is used in the receiver. A complete downlink is provided, including burst construction, 8PSK modulation, and synchronization.

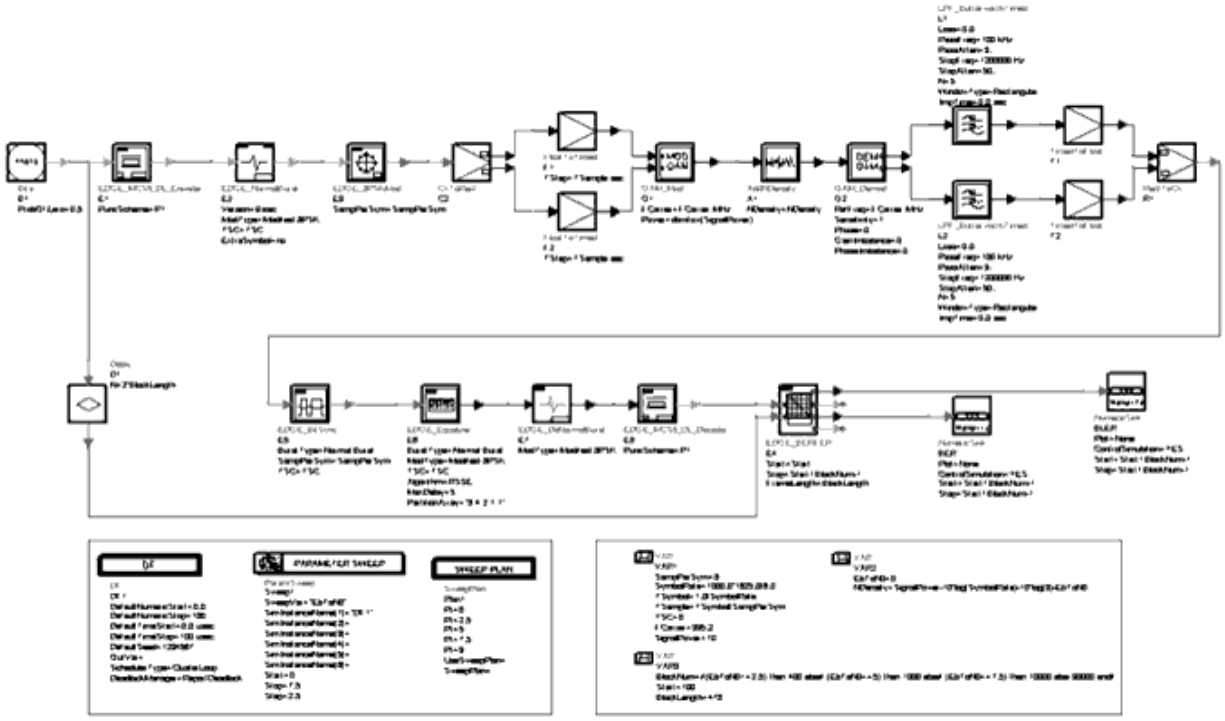
Compared to data from Nokia and Ericsson, the ADS receiver has the same performance as uncoded (without channel coding) BER/BLER, but 1~2 dB worse as coded (with channel coding) BER/BLER. This 1~2 dB difference (described in the *Results Analysis* section) results mainly from the adaptive equalizer used by ADS EDGE and the equalizers used by Nokia and Ericsson.

Schematic Examples

The MCS5_Static_AdaptiveEq is an example using an adaptive equalizer; the schematic is shown in the following figure.

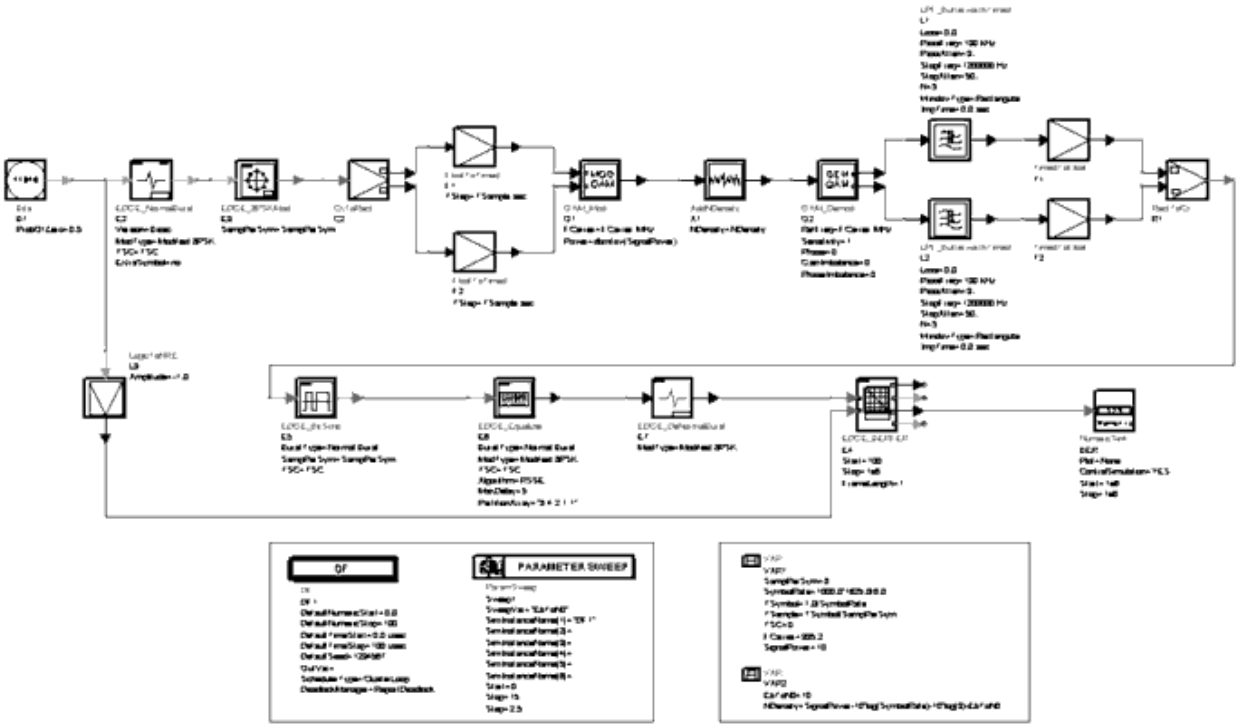
Bits acts as a data source that generates a random bit stream. EDGE_MCS5_DL_Encoder is used for channel coding. EDGE_NormalBurst is used to form the burst structure with the coded bits. EDGE_8PSKMod performs 8PSK modulation. The complex symbols after 8PSK modulation are converted to timed signal, QAM modulated, QAM demodulated and converted to complex symbols again. AddNDensity simulates the additive white Gaussian noise channel.

The signal passes through a Butterworth lowpass filter that acts as the receiving filter of the receiver. EDGE_BitSync is used for synchronization. EDGE_Equalizer performs adaptive equalization. EDGE_DeNormalBurst extracts useful data from the burst. EDGE_MCS5_DL_Decoder performs channel decoding. EDGE_BERFER calculates BER and FER(BLER).



MCS5_Static_AdaptiveEq

The Raw_Static_AdaptiveEq is the same as MCS5_Static_AdaptiveEq except channel coding and decoding are not included. The schematic is shown in the following figure.



Raw_Static_AdaptiveEq

Key parameter information for all designs is provided in the following table.

Key Parameter Information

Function Unit	Key Parameter	Setting	Description or Notes
RSSE Equalizer	PartitionArray	"84211"	partition array, to define the number of subsets used in each stage of RSSE. See the documentation of the model for detail.
Butterworth Filter	PassFreq	100 KHz	typical bandwidth for EDGE in baseband simulation
	N	5	order of this filter
AddNDensity	SignalPower	10	transmitted signal power, 0.01w, i.e. 10 dBm
	NDensity	SignalPower-10*log(SymbolRate)-10*log(3)-EbToN0	†
System Setting	SampPerSym	8	number of samples per symbol
	SymbolRate	1000*1625/6 symbol per second	EDGE symbol rate
† noise density calculation: see equations below this table.			

$$E_bToN_0 = \frac{SignalPower \times BitTime}{N_0} = \frac{SignalPower \times \frac{SymbolTime}{3}}{N_0} = \frac{SignalPower}{N_0 \times 3 \times SymbolRate}$$

$$N_0 = \frac{SignalPower}{E_bTo N_0 \times 3 \times SymbolRate}$$

$$N_0(dBm) = SignalPower(dBm) - 10 \times \log(SymbolRate) - 10 \times \log(3) - E_bTo N_0(dB)$$

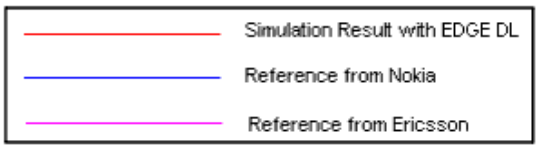
Reference Point

While ETSI doc 2e99-261 rev4 is the main specification for MCS models, the newer ETSI doc 2e99-999 is used in this workspace. Simulation results are the same.

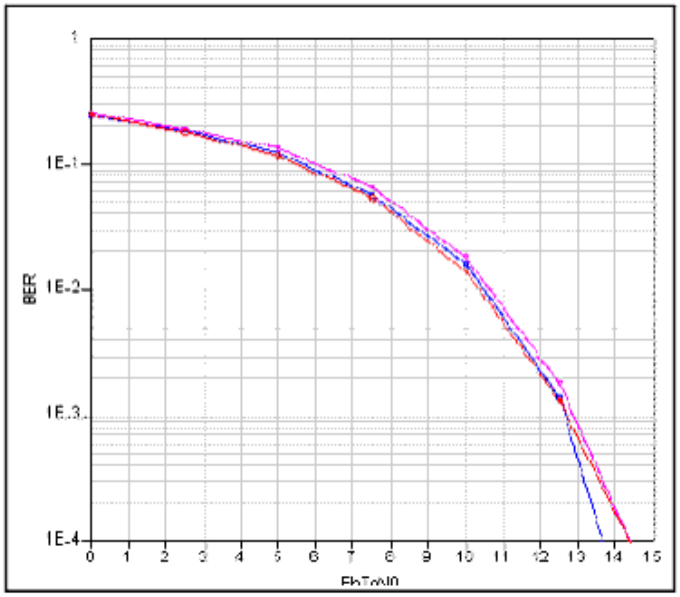
Nokia and Ericsson BER/BLER results are displayed for comparison in the ADS EDGE BER/BLER simulation results. Reference results of Ericsson are from Tdoc SMG2 EDGE 274/99(rev 2); Nokia are from Tdoc SMG2 EDGE XXX/99.

Simulation Results

The simulation results using the adaptive equalizer in a static channel for MCS5 through MCS9 and raw BER, including references from Nokia and Ericsson, are shown in the following six figures. The legend used in all results is shown in the first figure.

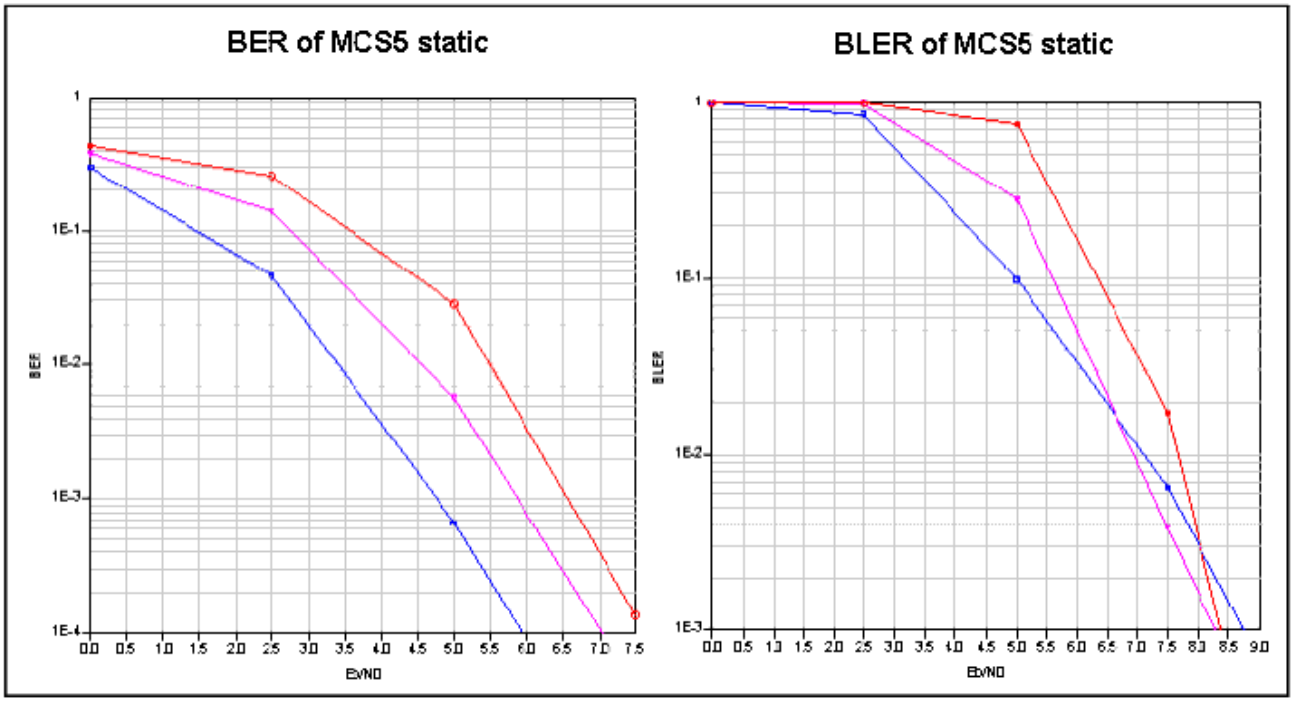


Legend

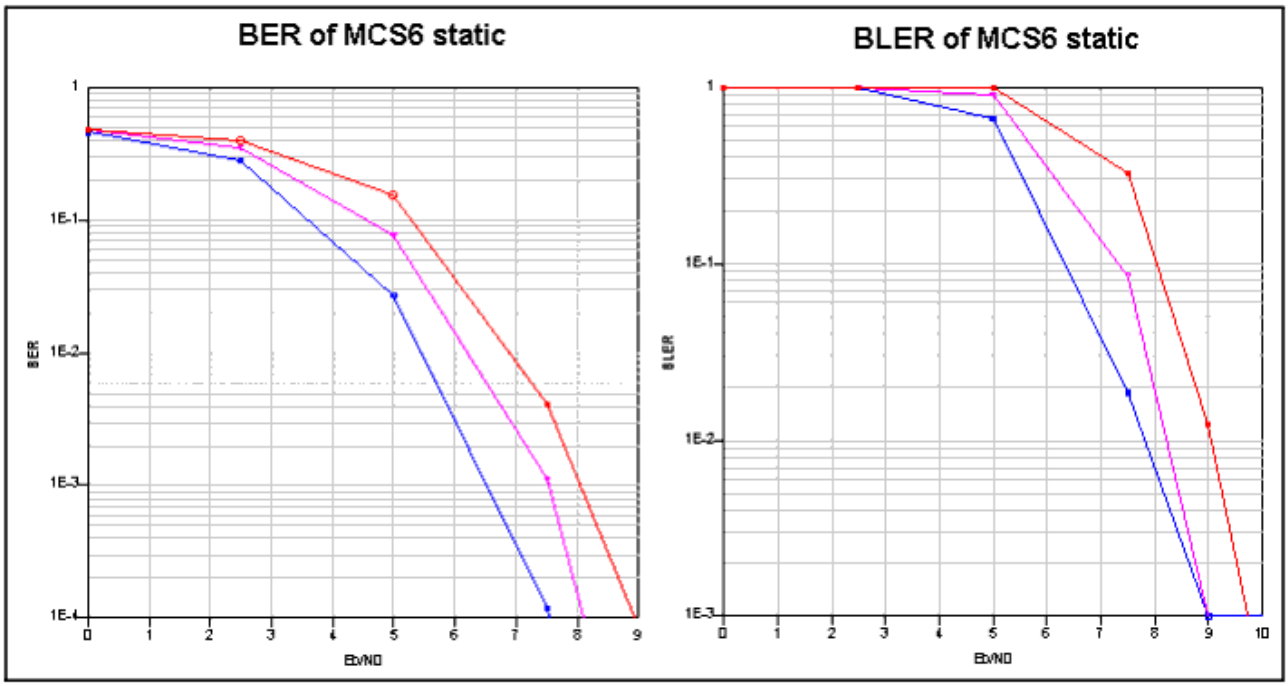


RSSE Adaptive Equalizer, Static Channel Raw BER

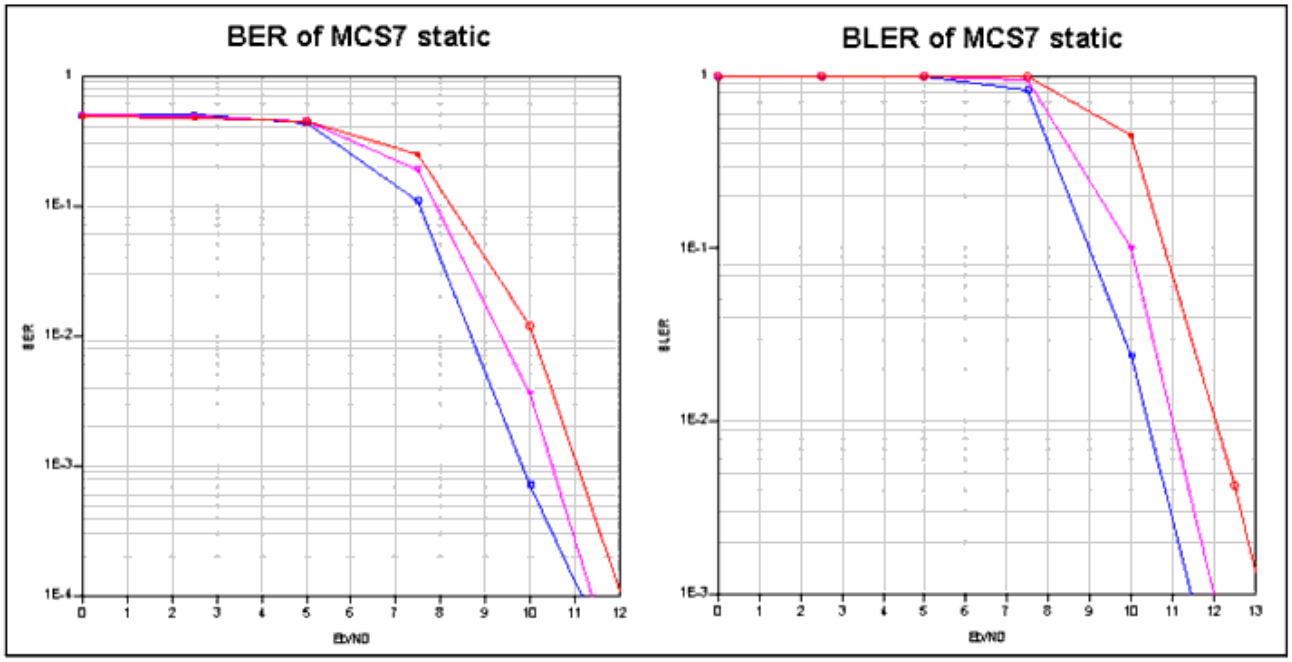
RSSE Adaptive Equalizer, Static Channel Raw BER



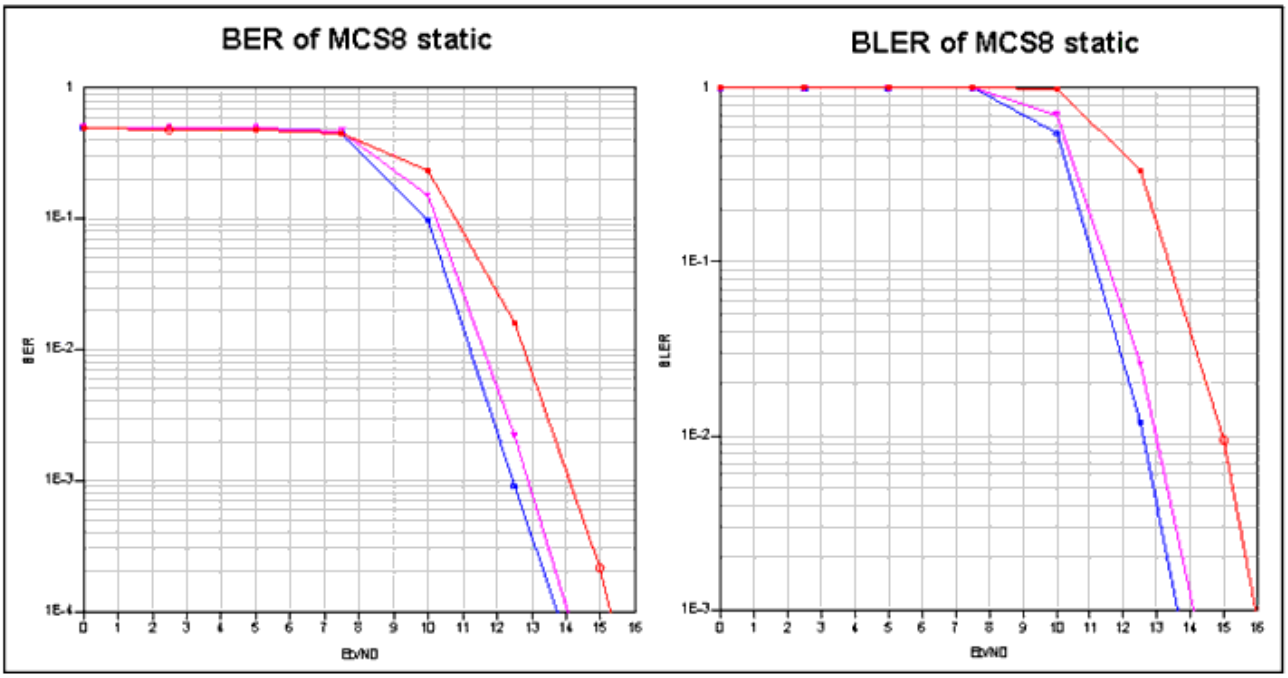
RSSE Adaptive Equalizer, MCS5



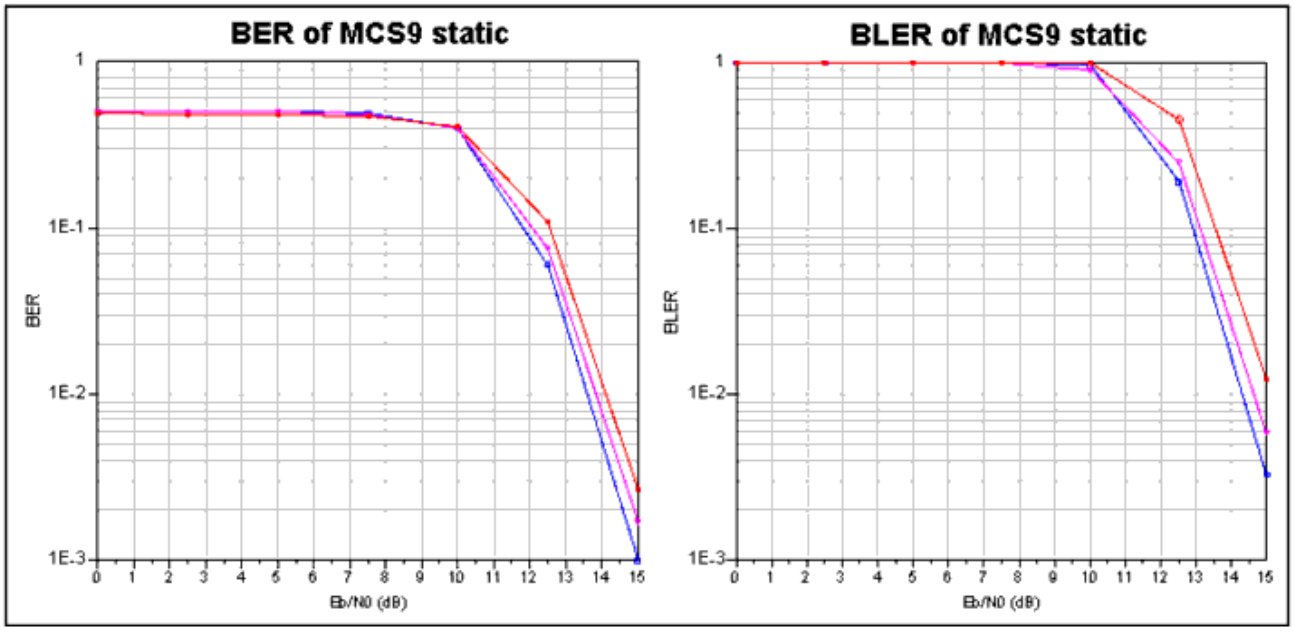
RSSE Adaptive Equalizer, MCS6



RSSE Adaptive Equalizer MCS7



RSSE Adaptive Equalizer MCS8



RSSE Adaptive Equalizer MCS9

Eb/No Differences Compared to ADS Simulation and Nokia or Ericsson Data, BER=1%

ADS Differences Compared to Nokia	ADS Differences Compared to Ericsson	
Raw	-0.13 dB	-0.29 dB
MCS5	2.08 dB	0.92 dB
MCS6	1.43 dB	0.68 dB
MCS7	1.38 dB	0.73 dB
MCS8	1.57 dB	1.17 dB
MCS9	0.52 dB	0.28 dB

Eb/No Differences Compared to ADS Simulation and Nokia or Ericsson Data, BLER=10%

ADS Differences Compared to Nokia	ADS Differences Compared to Ericsson	
MCS5	1.34 dB	0.72 dB
MCS6	1.73 dB	0.72 dB
MCS7	1.80 dB	0.80 dB
MCS8	2.24 dB	1.86 dB
MCS9	0.65 dB	0.43 dB

This BER validation workspace shows that simulation results without channel coding (uncoded) are as good as that of Ericsson and Nokia, and simulation results with channel coding (coded) are 1~2 dB worse (except, MCS9 code rate is 1) compared to Ericsson and Nokia.

Differences described above are because of equalizer performance and the fact that the adaptive equalizer used in this workspace has hard-decision output while Ericsson and Nokia equalizers are assumed to have soft-decision output. The Results Analysis section describes these differences.

Benchmark

- Hardware Platform: Pentium III 1000 MHz, 512 MB memory
- Software Platform: Windows 2000, Advanced Design System 1.5

Results Analysis

Uncoded simulation does not use Viterbi decoding and the equalizer output will be used for the final BER calculation. Therefore, equalizer hard- or soft-decision does not impact system performance. In coded simulation, Viterbi decoding receives input from the equalizer; soft-decision equalizer output has a gain of 1~2 dB compared to hard-decision equalizer output. Given these facts, simulations in this workspace perform as good as Ericsson and Nokia in the uncoded condition, but not as good when channel coding/decoding is used.

Codec designs provided with this workspace are used to demonstrate the accuracy of the ADS EDGE coder/decoder, and that the 1~2 dB differences in coded simulation are caused by the different hard- or soft-decision outputs of the equalizer (the input to the Viterbi decoder). These designs include:

- Codec_MCS5_DL
- Codec_MCS6_DL
- Codec_MCS7_DL
- Codec_MCS8_DL
- Codec_MCS9_DL

Features used for the analysis include:

- Coding and Decoding
- Via Baseband AWGN Channel
- Performance comparison of hard-decision and 4-bit-soft-decision input to the decoder
- MCS5 through MCS9

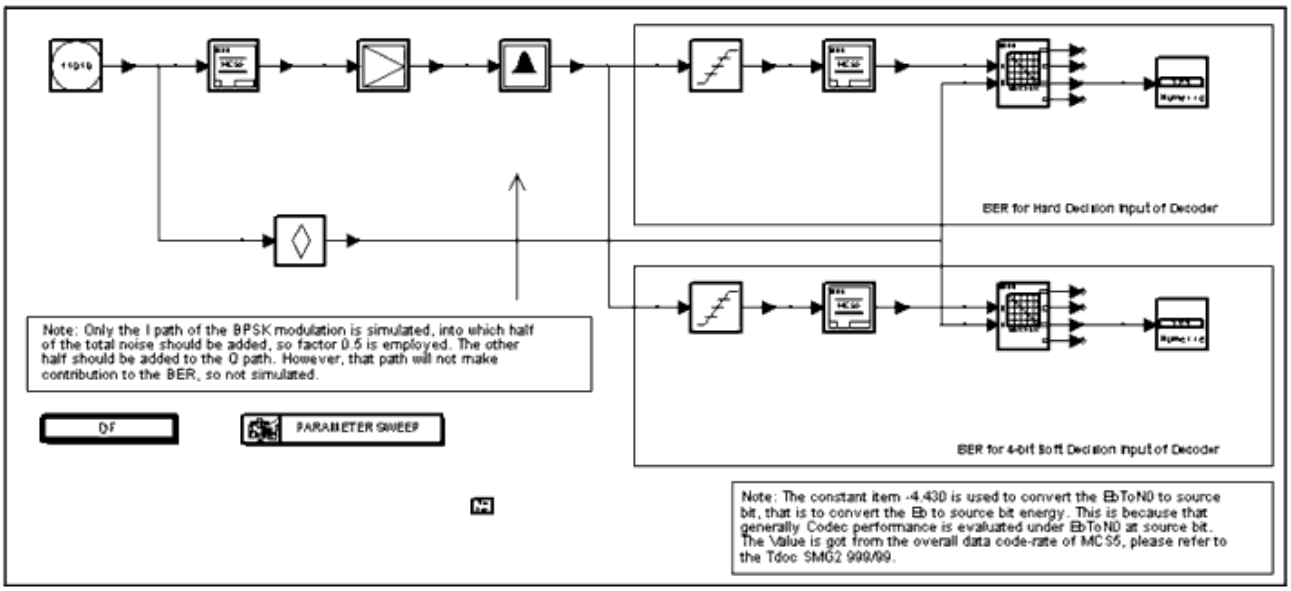
Downlink encoding is used in the designs, then noise is added. At the decoding end, received data is split into two paths for hard- and soft-decision. 4-bit uniform quantization is used to implement the soft-decision. Decoders are used for each path; one has hard-decision input, one has soft-decision input. BER is measured and performances of the two cases can be compared.

In the BER validation designs, the equalizer is located in front of the decoder; the output is the input of the decoder. So, the type of equalizer output determines whether the input of the decoder is hard- or soft-decision data.

In the Codec designs, the decoder is imported with hard- and soft-decision inputs, and the BER of both cases are measured. In this setup, simulation results indicate the Codec performance under the two conditions. If the differences in these designs are similar to those in the coded case in the BER validation designs, the above conclusion can be verified. That is, the 1~2 dB differences in the coded simulation in BER validation designs are caused by the different (hard- or soft-decision) output of the equalizer.

Schematic Examples for Codec Designs

The Codec_MCS5_DL schematic is shown in the following figure as an example; MCS6 through MCS9 schematics are similar.



Codec_MCS5_DL Schematic

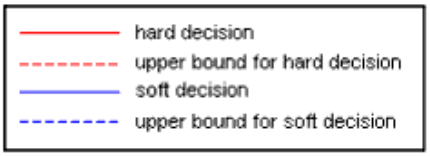
In the schematic, random source data is encoded by the MCS5 downlink encoder. The LogicToNRZ converter converts the coded 0 and 1 to 1 and -1, respectively; it can be regarded as the I path of a BPSK modulator. The Q path of the simulator is omitted, for it will make no contribution to the BER measurement. Noise is added in the AWGN_Channel. Since signal power is 1, the noise variance of the AWGN_Channel can easily be calculated from EbToN0. A factor of 0.5 is used when adding the noise, because another half of the total noise should be added into the Q path, which is omitted. At the decoding end, data is split into two paths; the upper path is for hard-decision, the lower path is for soft-decision. 4-bit uniform quantization is used in the lower path to implement the soft-decision. Decoding and BER measurement are performed in each path.

The following table lists key parameter and variable settings in Codec designs.

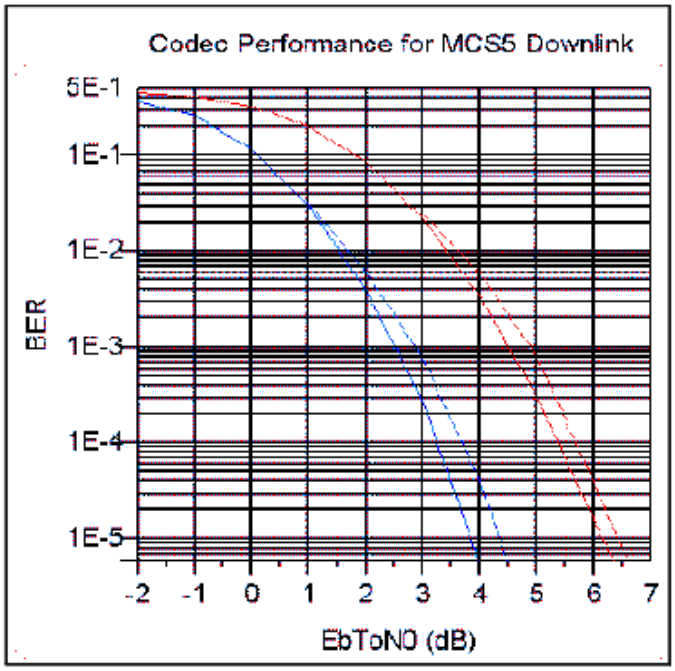
Key Settings in Codec Designs

Parameter/Variable	Settings	Comments
NoisePwr	1.0/(10^((EbToN0-X)/10))	†
Thresholds in Quant	-1.75 -1.5 -1.25 -1.0 -0.75 -0.5 -0.25 0.0 0.25 0.5 0.75 1.0 1.25 1.5 1.75	15 thresholds for 4-bit uniform quantization
†EbToN0_tb=SNR, where EbToN0_tb denotes the EbToN0 at transmitted bit; so NoisePwr=(Signal Power)/EbToN0_tb;An adjust item X is used to convert the EbToN0_tb to source (before encoding) bit, that is to convert the Eb to source bit energy. This is because that generally Codec performance is evaluated under EbToN0 at source bit. EbToN0=EbToN0_tb+X, and thus, EbToN0_tb=EbToN0-X. The Value of X is derived from the overall data code-rate of a given MCS, and varies for different MCSs; refer to [1].		

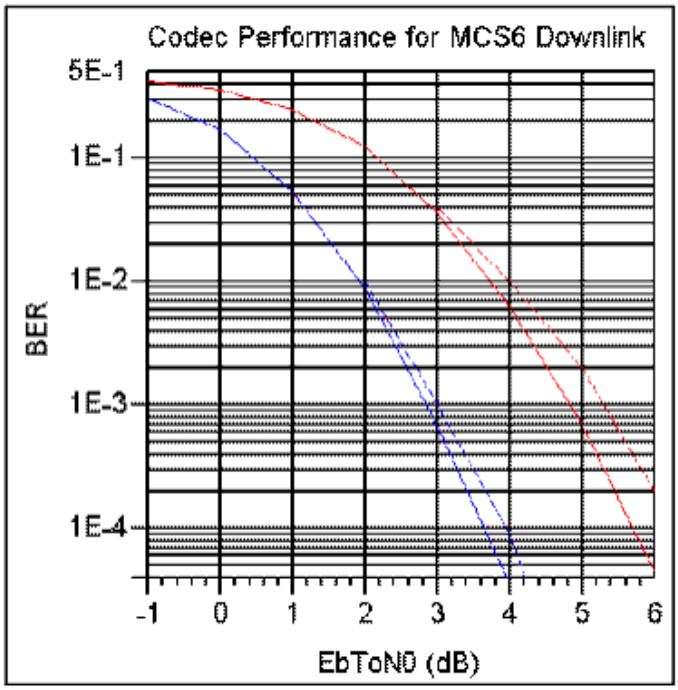
Simulation results for MCS5 through MCS9 are shown in the following five figures. The legend for these figures is shown in the first figure.



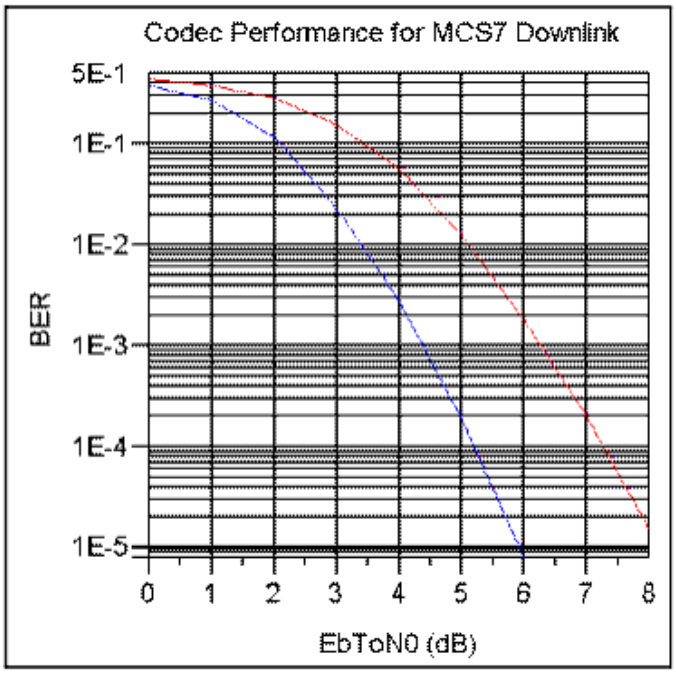
Legend



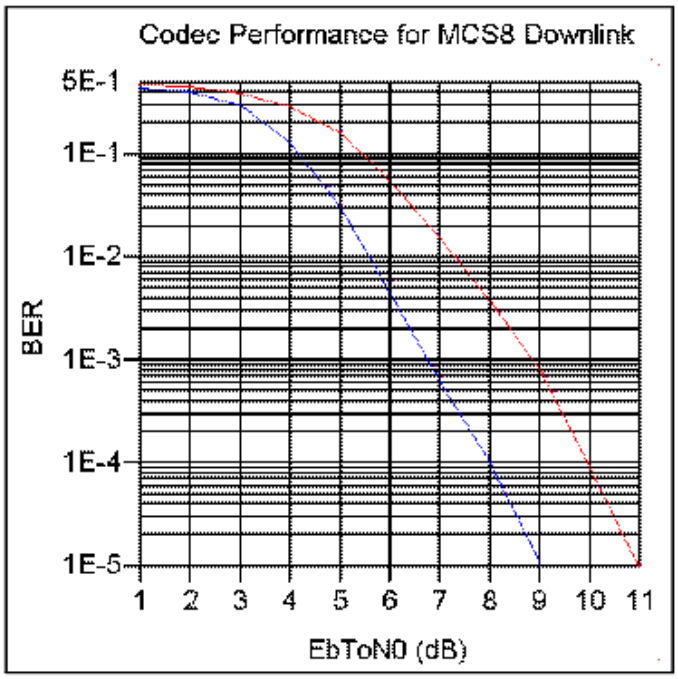
Codec Performance for MCS5 Downlink



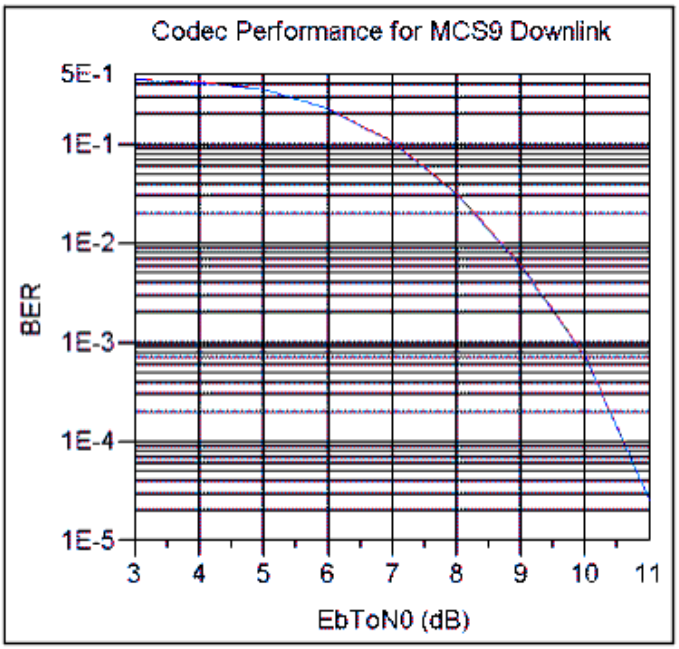
Codec Performance for MCS6 Downlink



Codec Performance for MCS7 Downlink



Codec Performance for MCS8 Downlink



Codec Performance for MCS9 Downlink

These results show performance differences between hard- and soft-decision. Trends on how hard- and soft-decision impact coding schemes MCS5 to MCS9 can easily be seen even though BPSK modulation is used instead of 8PSK modulation.

For MCS9 (code rate 1), curves for hard-decision and soft-decision are very close to

overlapping because soft-decision cannot benefit from zero-coding gain. As expectd, the ADS BER performance for MCS9 is very close to data from Nokia and Ericsson.

It can be seen that carefully designed equalizers can improve receiver performance. There are dashed lines in the plots of MCS5 and MCS6 for the upper BER boundary in theory [4]. The mother code of all schemes (MCS5-MCS9) is a 1/3 convolutional code with a constraint length of 7.

After puncturing, each scheme has its own code rate. In MCS5, little puncturing is used so its code rate is close to 1/3; the upper boundary curve used in the plot is the 1/3 convolutional code with a constraint length of 7. After puncturing, the code rate of MCS6 is close to 1/2, so the upper boundary curve used in it is the 1/2 convolutional code with a constraint length of 7. It can be seen that the simulation results in both schemes are within the boundary.

Benchmark for Codec Designs

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT, Advanced Design System 2001

References

1. Tdoc SMG2 EDGE 999/99, CR 05.03-A025 EGPRS Channel coding, September 1999.
2. Tdoc SMG2 EDGE 274/99(rev 2), EGPRS Receiver Performance, Ericsson, August 1999.
3. Tdoc SMG2 EDGE XXX/99, Performance Results for EDGE EGPRS 8PSK Transmission Schemes, Nokia, August 1999.
4. Proakis, J. G., *Digital Communications, Third Edition* , pp508, McGraw-Hill.

EDGE Design Examples

Introduction

The following design example workspaces are available with the EDGE software; the associated design examples are described in the following sections.

- 8PSK modulation spectrum: EDGE_8PSKMod_Spec_wrk
- RSSE equalizer performance: EDGE_Equalizer_wrk
- downlink modulating and coding scheme 1: EDGE_MCS1_DL_wrk
- downlink modulating and coding scheme 5: EDGE_MCS5_DL_wrk
- RF traffic channel measurements: EDGE_RF_Measurement_wrk
- error vector magnitude measurements: EVM_Examples_wrk

8PSK Modulation Spectrum

EDGE_8PSKMod_Spec_wrk Design Name

- EDGE_8PSKMod_Spec

Features

- 8PSK modulation with pulse shaping filter and continuous $\frac{3}{8}\pi$ symbol phase rotation
- adjustable sample rate
- spectrum analysis and constellation display
- integrated RF section
- EVM measurements

Description

This example demonstrates 8PSK modulation, a key feature of EDGE. The example includes 8PSK modulation, equalization, derotation, and RF. It shows constellations and other graphs in various phases of the modulation process. And, spectrum analysis is performed at IF and RF.

8PSK is a linear modulation, where three consecutive bits are Gray-mapped into one symbol on the I/Q axis, with a symbol rate of 270.833 kilosymbols per second. BitsToInt and TableCx models are used to accomplish Gray-mapping.

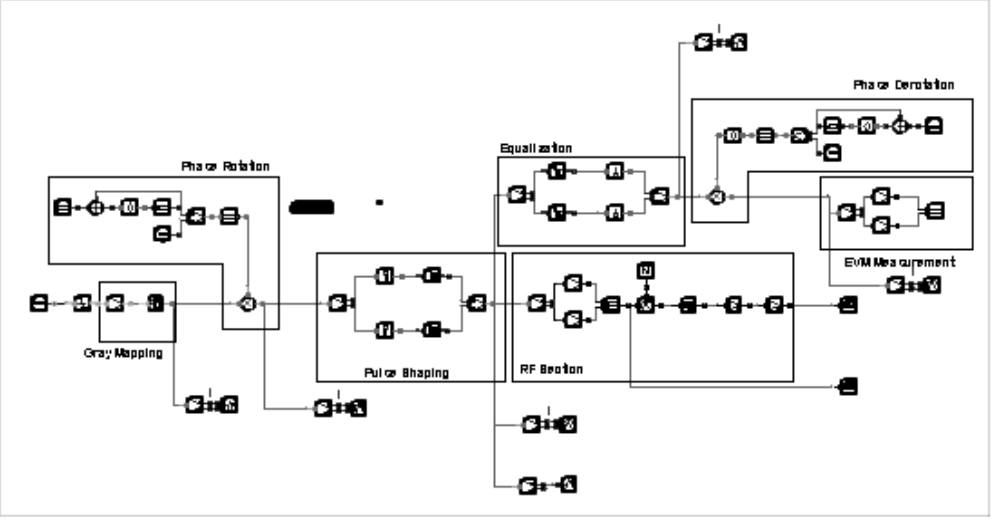
To avoid the envelope of modulated signals becoming zero, symbols are rotated by $\frac{3}{8}\pi$ radians per symbol; the constellation is not rotated and does not go through the origin. A sequence of complex exponential symbols is generated in the phase generation section to implement continuous $\frac{3}{8}\pi$ phase rotation. The phase generation section contains seven models and stretches its output to MpyCx2. A pulse-shaping filter is used to minimize the impact on the spectrum, especially for the adjacent channels. This filter is equal to the main component in the Laurant expansion of GMSK modulation (the Laurant expansion provides a method for expressing binary CPM signals as a sum of amplitude modulated pulses); its impulse response is *C* 0(*t*). After baseband modulation, the signal is fed into the RF section, which consists of RF mixer, Butterworth filter, and RF gains.

Equalization is made up of the demodulation filters. The demodulation filter frequency response is derived from the restriction that the frequency response of the cascade of the modulation and demodulation filters yields zero or controlled ISI (inter-symbol interference) at the sampling instants. An approximate raised-cosine spectrum with a 0 rolloff factor is used in practice for the spectrum of the cascade.

Schematics

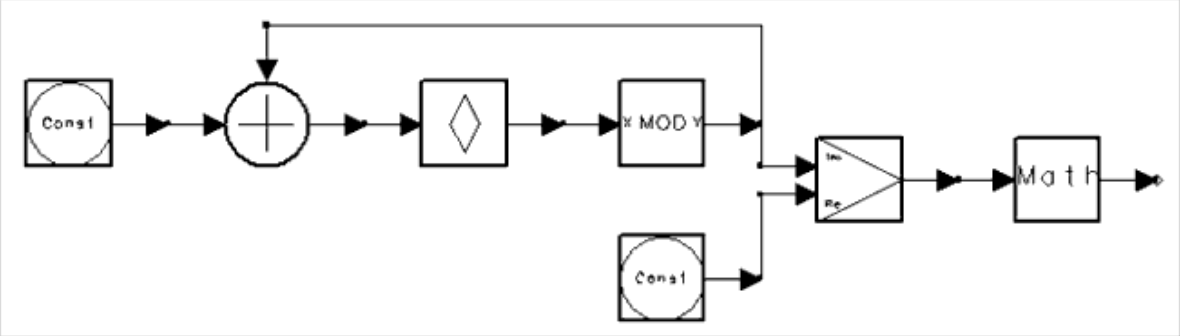
The following figure shows the schematic for this design. It contains random bit source, Gray-mapping, phase rotation, pulse shaping, RF, equalization, phase de-rotation, EVM measurement, and other measurement and display components.

- Gray-mapping consists of BitsToInt and TableCx models, which Gray-maps three binary bits to one symbol.
- Phase rotation generates a continuous increasing phase with a $\frac{3}{8}\pi$ step and rotates the Gray-mapped symbol with this phase.



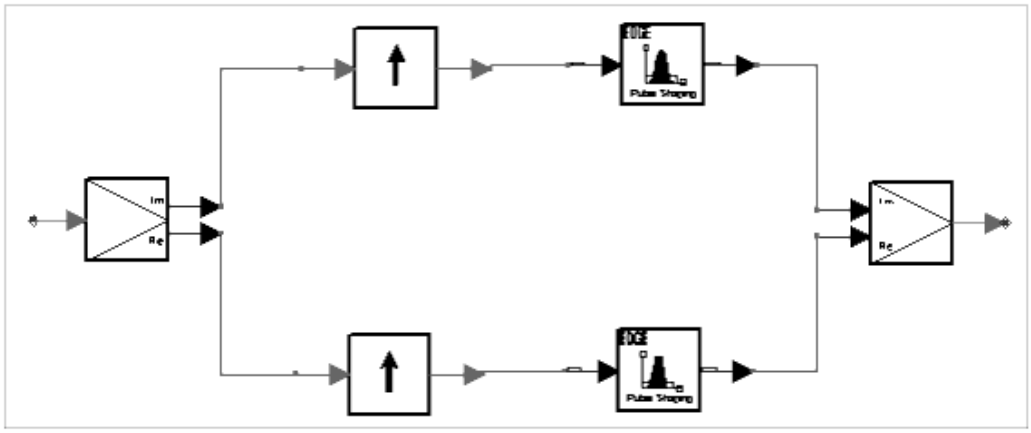
EDGE_8PSKMod_Spec Schematic

- The following figure illustrates phase generation. It generates the complex exponential symbols $e^{jn3\frac{\pi}{8}}$ using a Const source followed by an accumulator.



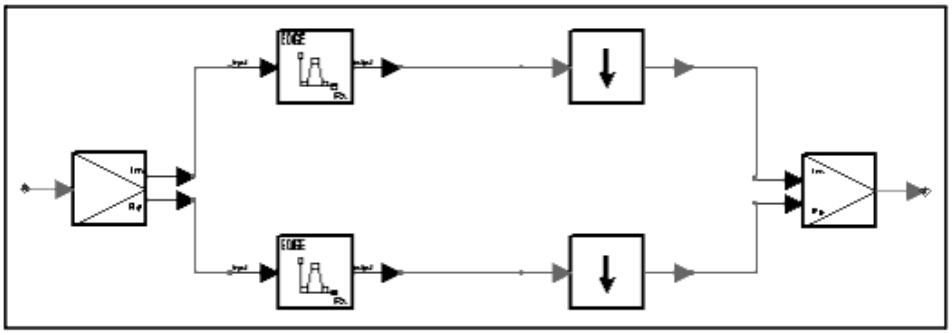
Phase Generation Schematic

- Pulse shaping pulse shapes the symbols in both real and image parts, using the pulse shaping filter EDGE_PulseShapingFltr. The following figure shows the pulse shaping schematic. The CxToRect model converts the complex signal into real signals and the signals are upsampled and pulse shaped in both the real and imaginary parts. EDGE_PulseShapingFltr is built for the pulse shaping filter, and the filter's impulse response h(t) is *C* 0(*t*).



Pulse Shaping Schematic

- RF carries out radio-frequency modulation.
- The following figure shows the equalization section. Equalization suppresses the ISI at the sampling points, the value of which is determined by DownSample.



Equalization Schematic

Symbol	Specification	Simulation Type	Value
SampPerSym	number of samples in one symbol	Ptolemy	48
SymNum	impulse response length of demodulation filter in symbol unit	Ptolemy	31
Order	log base 2 of FFT transform size	Ptolemy	14
IRLength	impulse response length of demodulation filter in sample unit	Ptolemy	SymNum×SampPerSym
Delay	number of samples of delay in demodulation	Ptolemy	(IRLength+SampPerSym×5)/(2×SampPerSym)−1

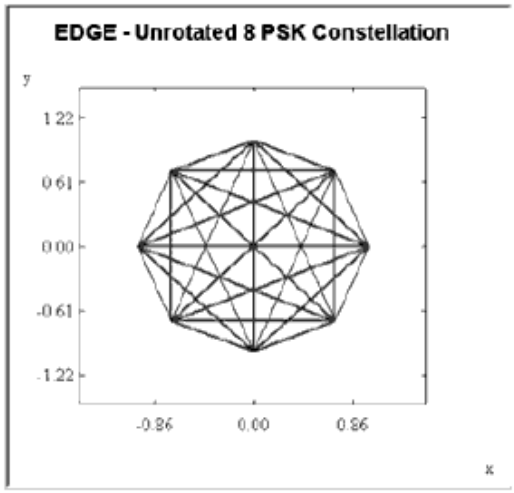
Notes

If SymNum is not odd, an incorrect delay value and simulation results will result.

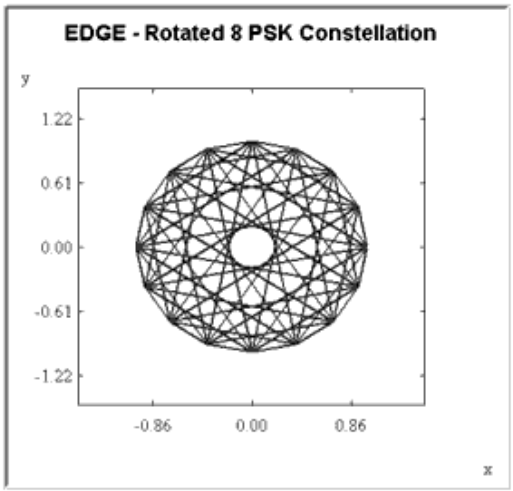
To improve demodulation performance, or reduce the ISI, increase IRlength and SymNum.

Simulation Results

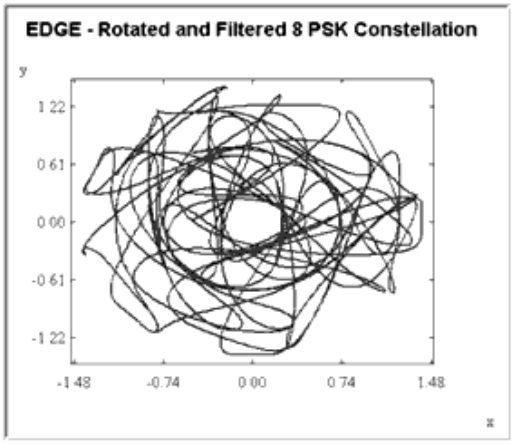
The following diagram shows the unrotated, rotated, and rotated and filtered constellations of EDGE 8PSK modulation. After rotation, the phase trajectories do not go through the origin and eight new states are generated.



Constellation of Unrotated 8PSK



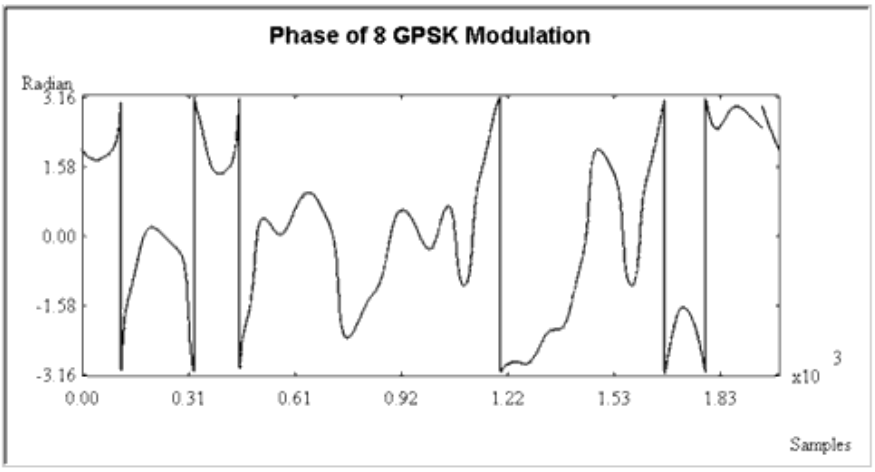
Constellation of Rotated 8PSK



Constellation of Rotated and Filtered 8PSK

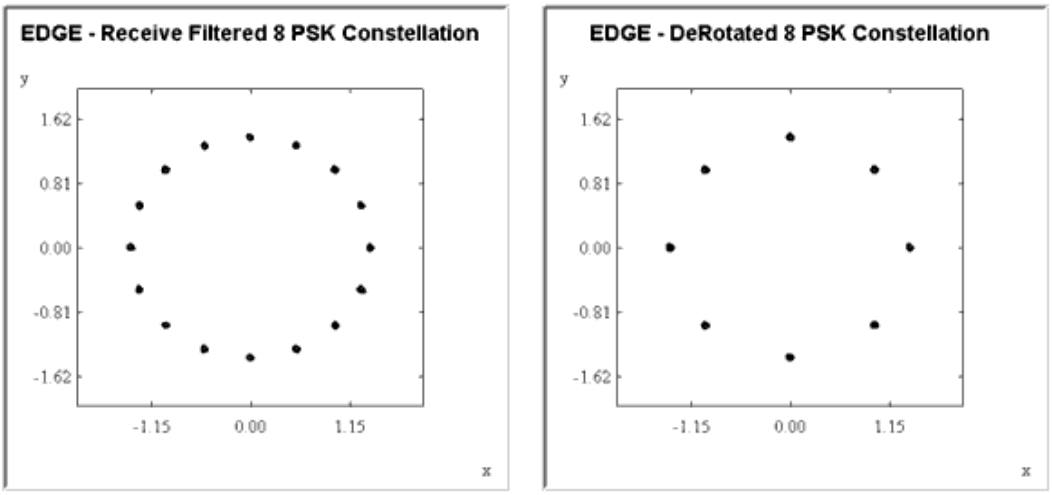
Constellations of EDGE_8PSK Modulation

The following figure shows the phase of 8PSK symbols vs. samples



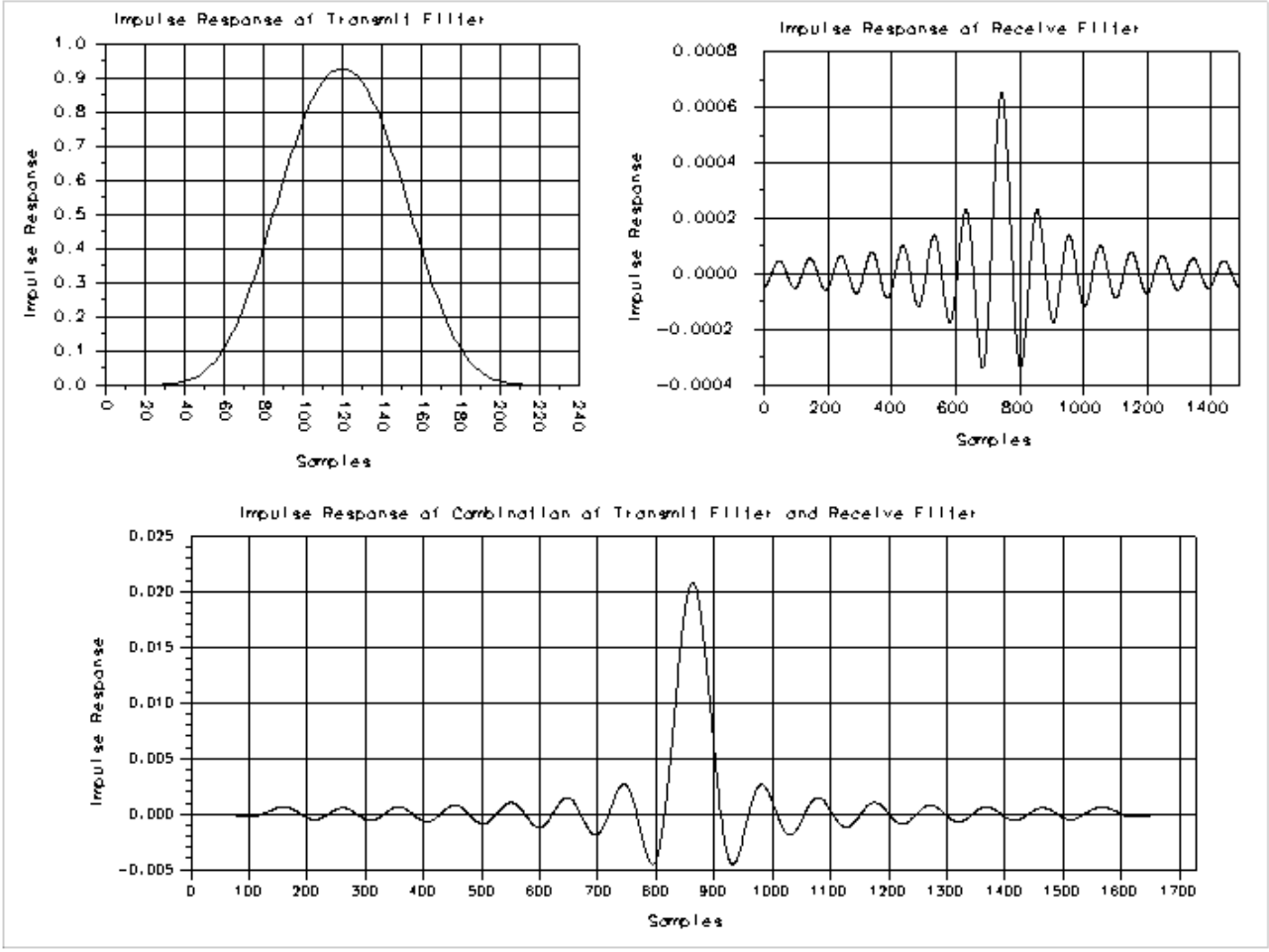
Phase of EDGE_8PSK Symbols

The following figure shows the demodulation filtered and de-rotated 8PSK demodulation constellations. Unlike modulation, the linking lines between adjacent symbols are not shown. Since the impulse response of the demodulation filter is a time finite sequence, zero ISI is unavailable and the symbols are slightly scattered around the points of desired states.



Demodulation Filtered and De-rotated Constellations

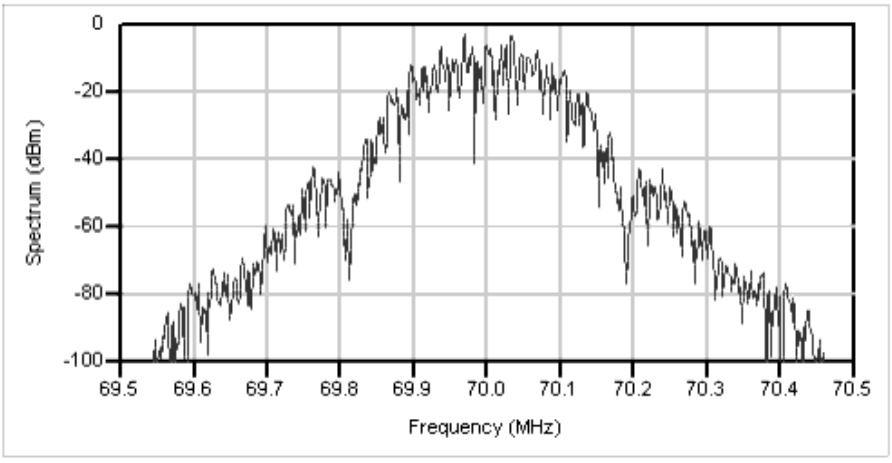
The following figure shows the impulse responses of modulation and demodulation filters, and the cascade of these filters. The impulse response of the modulation filter is *C* 0(*t*). The cascade has maximum magnitude at the sampling point and very small (approximately 0) magnitude at the sampling point of adjacent symbols, approaching zero ISI. The units of x and y axes are sample and magnitude for all three plots.



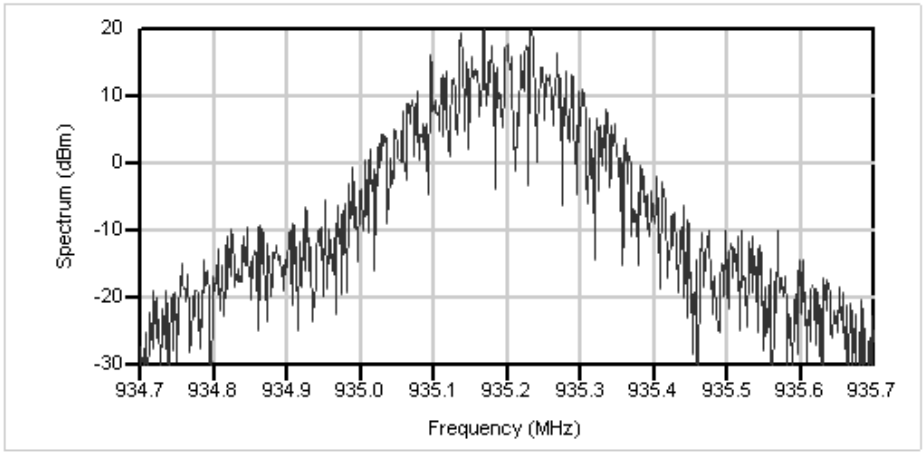
Impulse Response of Modulation, Demodulation Filters and their Cascade

The following two figures show the spectrum of 8PSK IF and RF modulated signals.

The EVM of the 8PSK modulated signal is 0.3%; the EVM is not zero because the EDGE_RxFilter used as an equalizer can only eliminate part of the ISI introduced by linearized Gaussian pulsing filter.



Spectrum of EDGE 8PSK IF Modulation



Spectrum of EDGE 8PSK RF Modulation

Benchmark

- Hardware platform: Pentium II 400 MHz, 256 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 156 × SampleRate
- Simulation time: 72 seconds

RSSE Equalizer Performance

EDGE_Equalizer_wrk Design Name

EDGE_EquPerform

Features

- 8PSK modulation with pulse-shaping filter and continuous $\frac{3}{8}\pi$ symbol phase rotation
- framed user data
- adjustable sample rate
- integrated RF section and GSM fading channel
- bit synchronization and RSSE equalization
- average received signal power measurements
- BER versus Eb/N_0 ratio

Description

This example demonstrates the performance of the reduced-state sequence estimation (RSSE) equalizer used in EDGE receiver in fading channel.

To eliminate inter-symbol interference (ISI) introduced by 8PSK modulation and channel memory, an equalizer is needed in the receiver. In the GSM Design Library, an adaptive equalizer that uses maximum likelihood sequence estimation (MLSE) algorithm was developed. Because of 8PSK modulation, an RSSE equalizer is used in the EDGE Design Library instead of an MLSE equalizer.

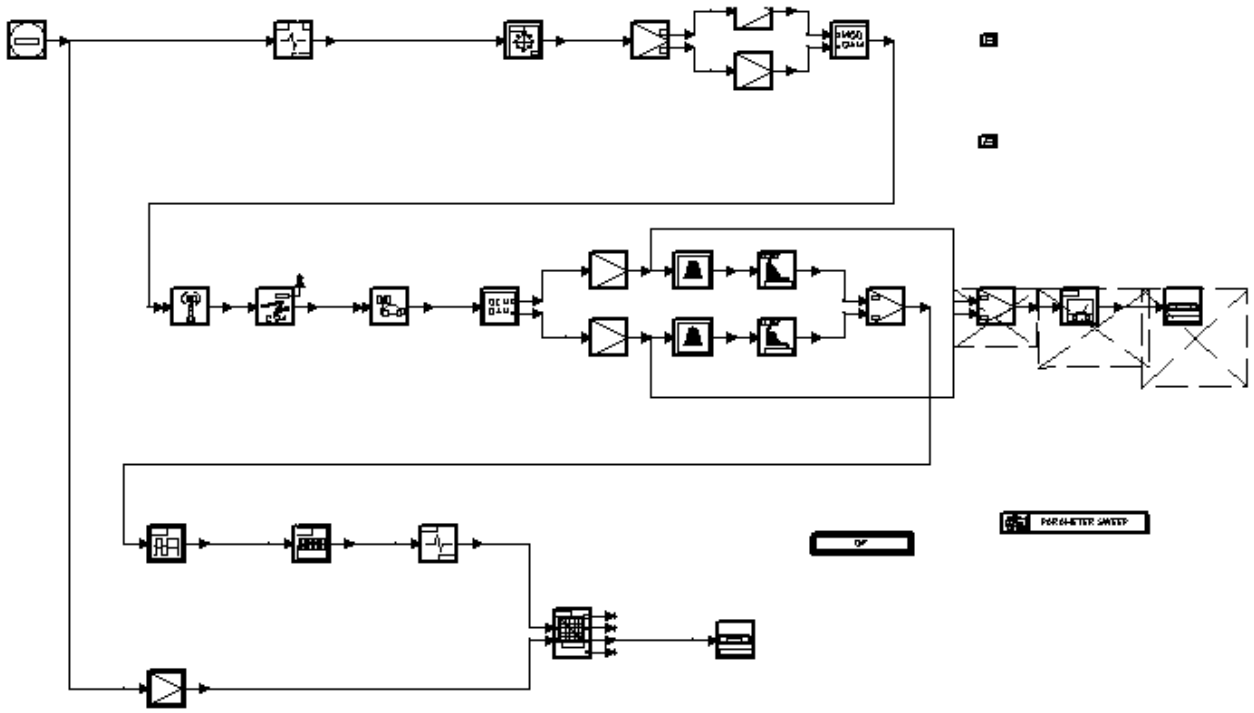
In the example design, user data is framed into normal bursts and then modulated by the 8PSK modulator EDGE_8PSKMod. The 8PSK modulated signal is modulated to RF (935.2 MHz) and passed through the GSM fading channel.

In the receiver, the input signal is demodulated to baseband, and bit synchronized by EDGE_BitSync. The bit-synchronized and downsampled data is then input to the RSSE equalizer EDGE_Equalizer. The equalizer performs channel estimation, matched filtering and adaptive equalization with Viterbi algorithm. The output of the equalizer is de-framed and compared with source data. BER performance is measured.

The channel model used here is TU50, an urban area mobile station moving at 50 km/hr. The disabled components in EDGE_EquPerform are used to measure the received signal power. By setting the Eb/N_0, the power of AWGN defined by NoisePwr in VAR is calculated by an equation. Thus, the BER performance to a certain Eb/N_0 can be obtained. The Eb/N0 in this example is swept from 10 dB to 20 dB in steps of 2 dB to obtain a curve of BER versus variable Eb/N_0.

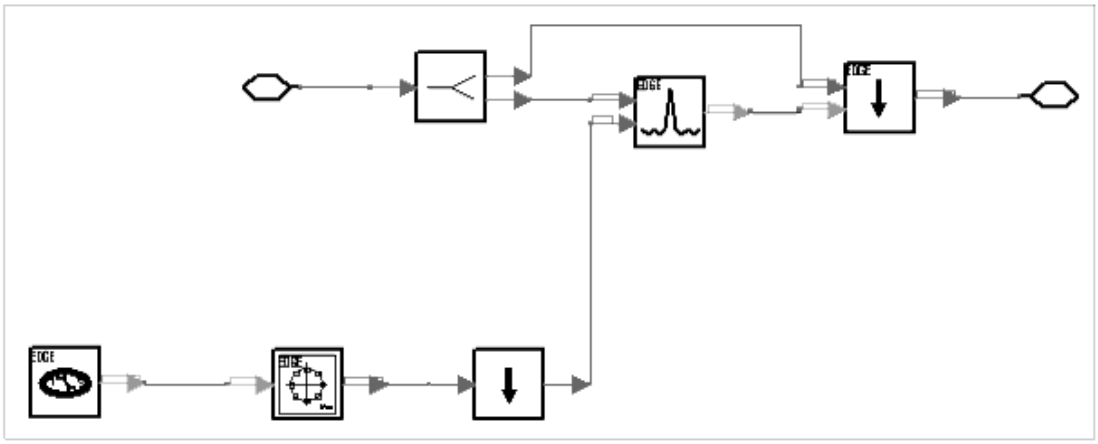
Schematics

The following figure shows the schematic for this design. It contains random bit sources, normal burst construction, 8PSK modulation, RF section, fading channel, additive white Gaussian noise, bit synchronization, RSSE equalizer, normal burst disassembly and BER measurement. The disabled components are used to measure the received signal power.



EDGE_EquPerform Schematic

The following figure shows the bit synchronization schematic. It consists of training sequence generation, 8PSK modulation, phase recovery and down sampler. The phase recovery component implements correlation calculation between the input signal and locally modulated training sequence to determine the time delay and optimum downsampling phase. Using the output of phase recovery, the downsampler performs optimum downsampling and delay adjustment.

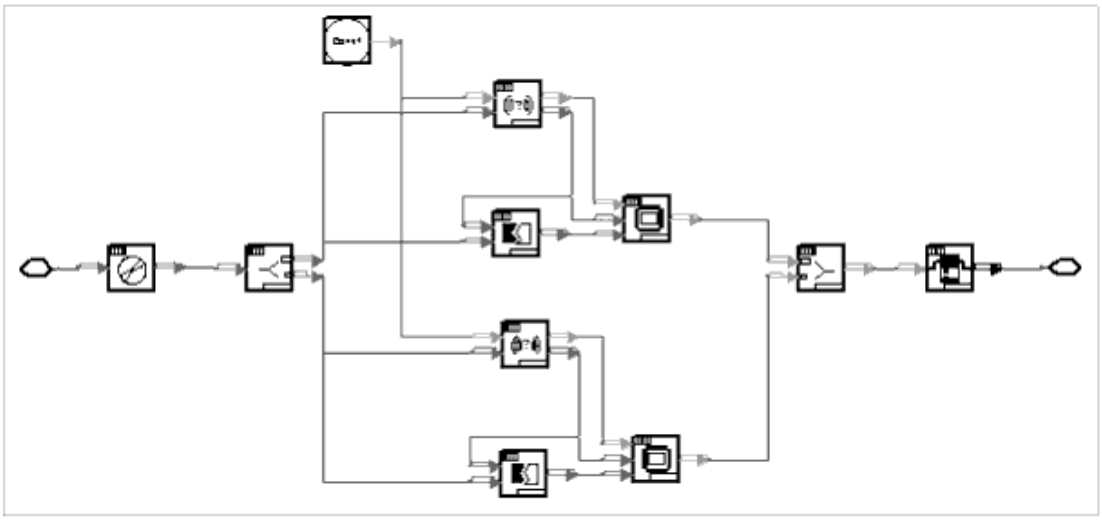


Bit Synchronization Schematic

The following figure shows the RSSE equalizer schematic. It consists of derotation, burst splitting, channel estimation, matched filtering, Viterbi algorithm processor, burst combining and state-to-float converter.

The phase de-rotator is used the eliminate cumulative $\frac{3}{8}\pi$ phase rotation. The de-rotated burst is split into two sub-frames for bidirectional equalization. Each sub-frame is matched-filtered with the coefficient provided by channel estimator. Channel estimation is performed using correlation characteristics of the training sequence.

The Viterbi algorithm processor is the core part of the equalizer. It implements the RSSE algorithm using the Ungerboeck state partition method and a modified Viterbi algorithm. It provides the hard decision results of state numbers of the 8PSK modulation; state numbers are then translated into bits by the state-to-float converter.



RSSE Equalization Schematic

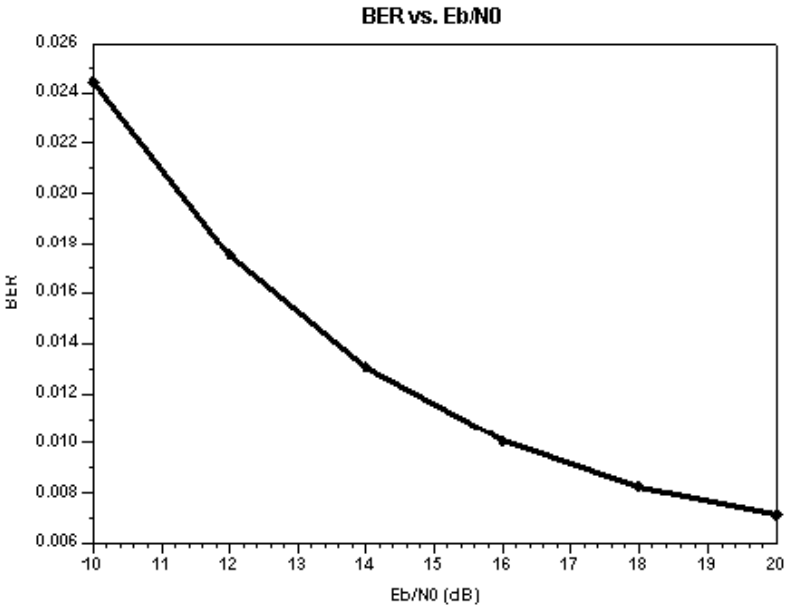
Symbol	Specification	Simulation Type	Value	Unit
SampleRate	number of samples in one symbol	Ptolemy	8	
SymbolRate	number of modulated symbols per second	Ptolemy	(1000.0×1625.0)/6	Hz
TSymbol	symbol interval	Ptolemy	1/SymbolRate	sec
FCarrier	carrier frequency	Ptolemy	935.2	MHz
TSC	training sequence code	Ptolemy	0	
Ps	average power of received signal	Ptolemy	0.4975311217	W
EbToN0	Eb/N0 ratio	Ptolemy	15	dB

Notes

- SampleRate must be an integer > 0.
- TSC can be an integer from 0 to 7.
- Ps must be the result of signal power measurement.
- NoiseVar (in VAR) noise power value can be calculated using EbToN0 and Ps with an equation.

Simulation Results

The following figure shows the equalizer performance BER vs. Eb/N_0.



Equalizer Performance BER vs. Eb/N_0

The following figure shows the numeric results of BER performance versus Eb/N_0.

BER vs. Eb/N0

EbToN0	BER[::,0]
10.0000000000	0.0244359756
12.0000000000	0.0175379825
14.0000000000	0.0130749869
16.0000000000	0.0100769899
18.0000000000	0.0082459918
20.0000000000	0.0071439929

Numeric Result of BER vs. Eb/N_0

Benchmark

- Hardware platform: Pentium Pro 200 MHz, 192 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 5 × 1e6
- Simulation time: 16 hours

Modulation and Coding Scheme 1 in Downlink

EDGE_MCS1_DL_wrk Design Names

MCS1_DL_HT100
MCS1_DL_PwrMeasure

Features

- GSM propagation fading channel and additive white Gaussian noise
- MCS-1 channel coding
- Channel interleaving and de-interleaving
- GMSK modulation and MLSE equalization
- Gaussian noise with adjustable noise variance
- BER and BLER performance measured versus variable Eb/N_0 ratio

Description

This example shows the system performance of BER and BLER for modulation and coding scheme 1 (MCS-1) in a downlink. It consists of error correction coding and decoding, interleaving and de-interleaving, data framing and deframing, GMSK modulation, GSM fading channel (RF section) and additive white Gaussian noise, bit synchronization and an equalizer with MLSE algorithm.

A random bit source is taken as user data source. The data is convolutionally coded at rate of 1/3, interleaved and fed into a normal burst construction component. After training bits, tail bits and guard time bits are added, data is placed in a GMSK modulation component. In this example only one user is considered.

The channel contains propagation fading channel and additive white Gaussian noise channel. Twelve channel types can be selected with adjustable parameters such as velocity, antenna height and location. In this example, the type propagation fading channel is HT100 (propagation fading model of hilly terrain and mobile station moving at radial speed of 100 km/hr).

In the receiver, the signal is filtered by a 7-pole Butterworth filter (in the GSM Design Library). The bit synchronization component is used to determine the time delay and optimum downsample phase, and performs delay adjustment and optimum downsampling. After signal recovery in the MLSE equalizer, burst disassembly, de-interleaving and channel decoding, BER and BLER are measured.

There are two designs in this example:

- MCS1_DL_PwrMeasure is used to measure the received signal power that will be used in calculating Eb/N_0 or SNR. The power measurement is performed by

  EDGE_SigPowerMeasure. It outputs the average signal power once each burst. The guard symbols in bursts are not counted in the average power.

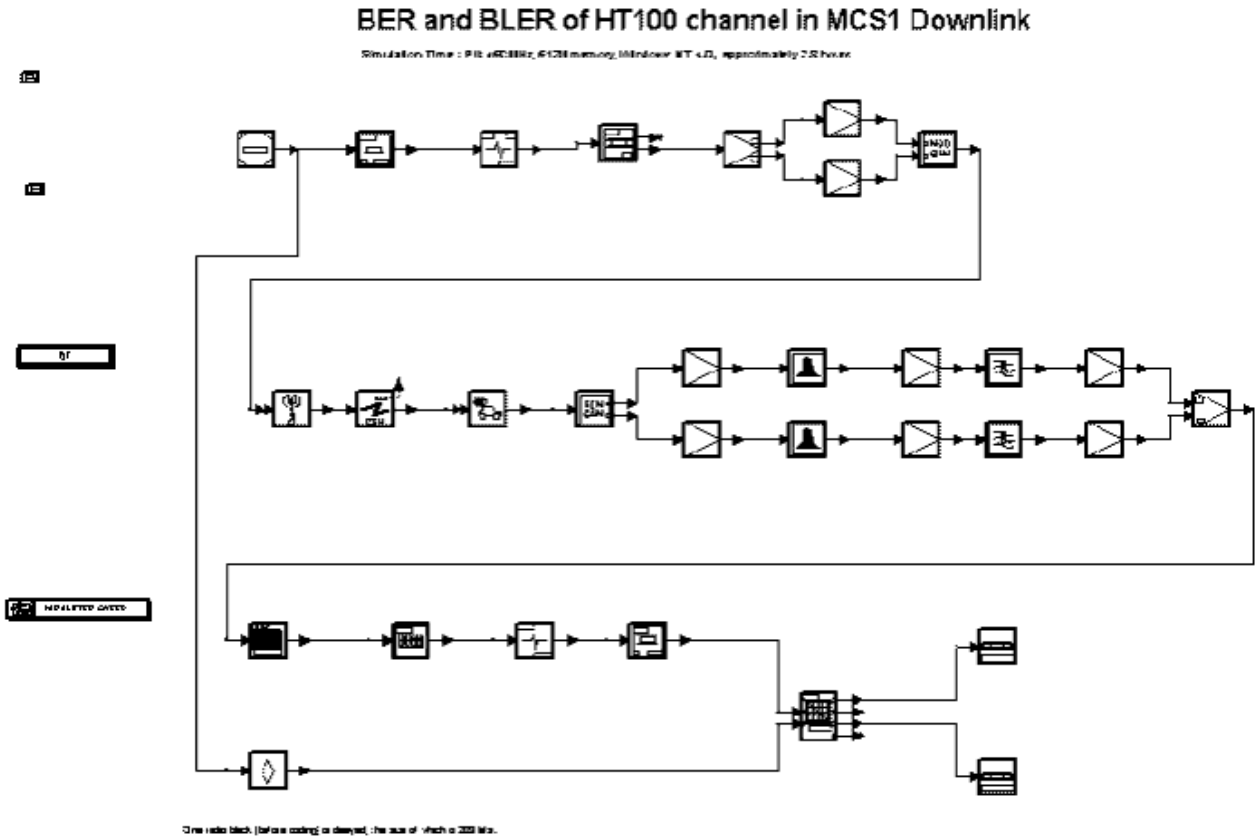
- MCS1_DL_HT100 is used to test BER and BLER over HT100 channel. The signal power measured in MCS1_DL_PwrMeasure is entered into VAR2.Ps. When EbToN0 of VAR2, for Eb/N_0, is set the power of noise is automatically calculated by an equation.

In this example, the value of Eb/N_0 is swept from 10 dB to 20 dB in 2 dB steps.

EDGE_BERFER is used to measure BER and BLER. Because there is a delay of one block in channel decoding, measurement starts from frame 1 and stops at frame 10001. Totally 10000 frames (10000 × 209 bits) are measured.

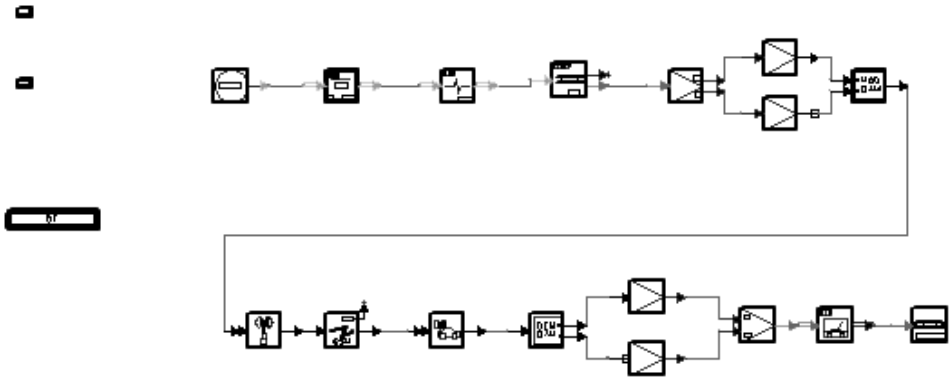
Schematics

The following figure shows the MCS1_DL_HT100 schematic. It contains random bit sources, normal burst construction, GMSK modulation, RF section, fading channel, additive white Gaussian noise, bit synchronization, MLSE equalizer, normal burst disassembly and BER and BLER measurement.



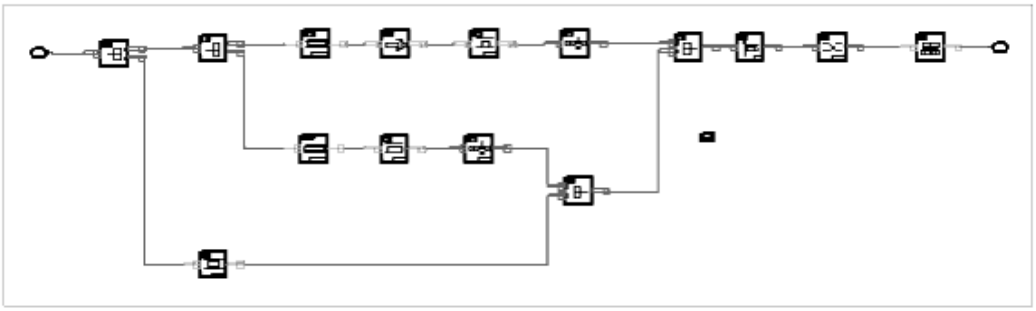
MCS1_DL_HT100 Schematic

The following figure shows the MCS1_DL_PwrMeasure schematic. Compared to the system design shown in the previous schematic, only the transmitter, propagation fading channel and AWGN channel are included; a receiver component is not applied. The average signal power measurement is performed at the input of the receiver by EDGE_SigPowerMeasure. It outputs results once each burst.



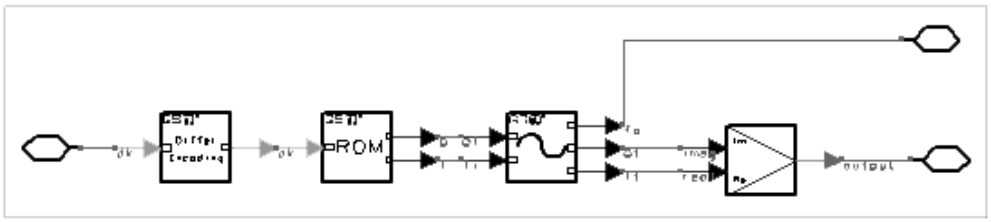
MCS1_DL_PwrMeasure Schematic

The following figure shows the EDGE_MCS1_DL_Encoder schematic used in this example. This subnetwork implements channel coding and interleaving of MCS1 in downlink. In each input data block of 209 bits, there are three USF bits, 28 header bits, and 178 data bits. The USF bits are pre-coded into 12 bits. Eight parity bits are added and convolutionally encoded with rate of 1/3 and constraint length of 7 and punctured, and the 28 header bits are encoded into 68 bits. Twelve parity bits are added to the 178-bit data block. By being convolutionally encoded and punctured, the 190-bit block results into a 372-bit block. The encoded USF, header and data bits are combined into a 452-bit block. Four extra stealing flag bits are then added. After an 8-bit coding scheme identifier is added, the data block has 464 bits. These final 464 bits are interleaved and mapped into four bursts.



EDGE_MCS1_DL_Encoder Subnetwork Schematic

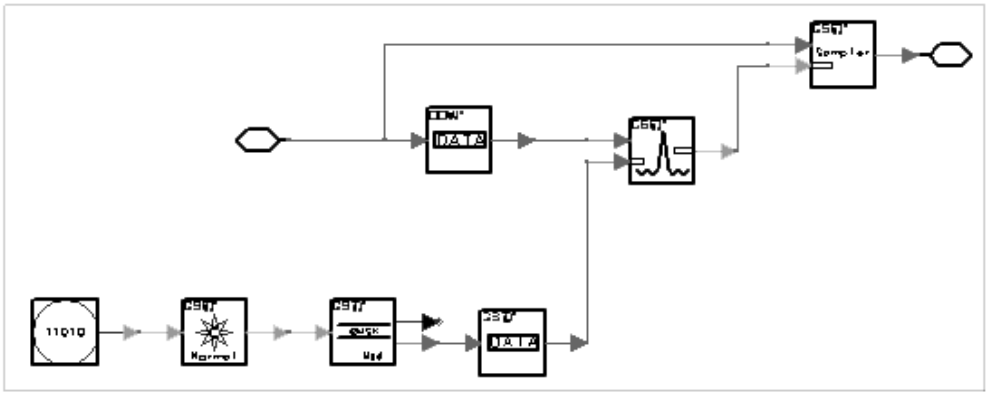
The following figure shows the GMSK modulator GSM_GMSKMod subnetwork schematic.



GSM_GMSKMod Subnetwork Schematic

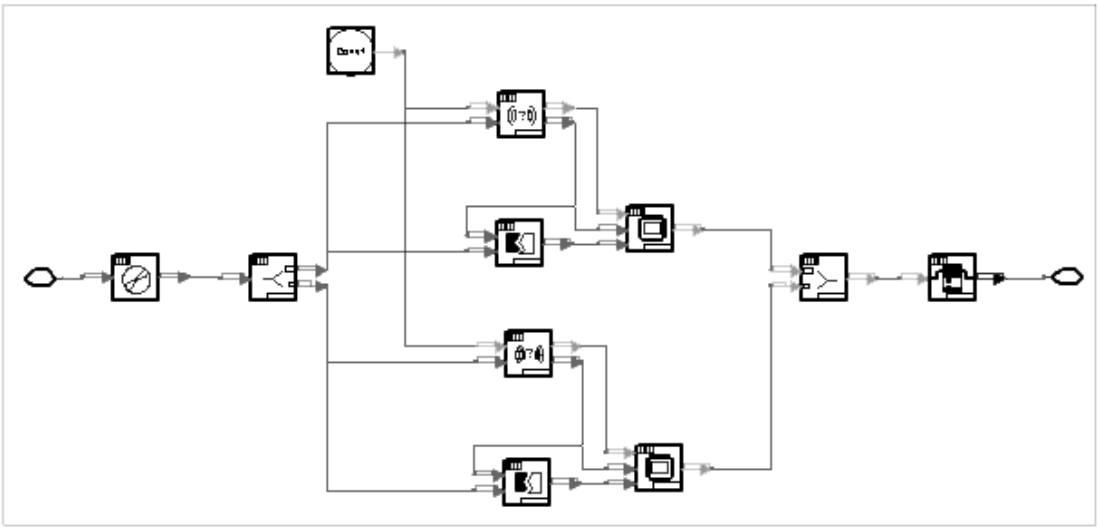
The following figure shows the bit synchronization subnetwork for normal burst. This GSM Design Library subnetwork consists of bit source, normal burst construction, GMSK modulation, data selection, phase recovery and downsampler. The phase recovery

component implements correlation calculation between the input signal and locally modulated training sequence to determine the optimum downsampling phase. Using the phase recovery output, the downsampler performs optimum downsampling to the input signal.



GSM_SynNBurst Subnetwork Schematic

The following figure shows the adaptive equalizer subnetwork. It implements the MLSE algorithm for GMSK modulation and reduced-state sequence estimation (RSSE) algorithm for 8PSK modulation. It consists of de-rotation, burst splitting, channel estimation, matched filtering, Viterbi algorithm processor, burst combining and state-to-float converter.



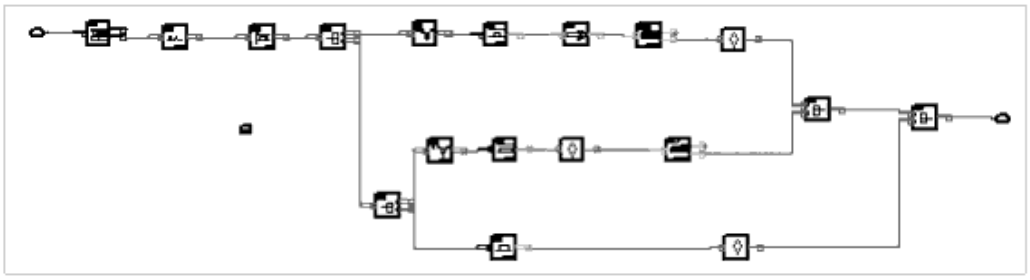
EDGE_Equalizer Subnetwork Schematic

The phase de-rotator is used the eliminate cumulative $\frac{3}{8}\pi$ phase rotation of 8PSK modulation or $\frac{\pi}{2}$ phase rotation introduced by differential encoding in GMSK modulation. The de-rotated burst is split into two sub-frames for bi-directional equalization. Each sub-frame is matched-filtered with the coefficient provided by channel estimation; channel estimation is performed using the correlation characteristics of the training sequence.

The Viterbi algorithm processor is the core part of the equalizer. It implements the RSSE

algorithm using the Ungerboeck state partition method and a modified Viterbi algorithm and the MLSE algorithm. It gives the hard decision results of state numbers of 8PSK or BPSK modulation. State numbers are then translated into bits by the state-to-float converter.

The following figure shows the MCS1 downlink channel decoding subnetwork. It consists of burst de-mapping, de-interleaving, extra stealing flag bits removing, de-puncturing, Viterbi decoder, and cyclic code decoder. Because there is a delay of five times the constraint length introduced by EDGE_ViterbiBitDCC, extra delays are needed. The final output of the channel decoder has a delay of one block, 209 bits.



EDGE_MCS1_DL_Decoder Subnetwork Schematic

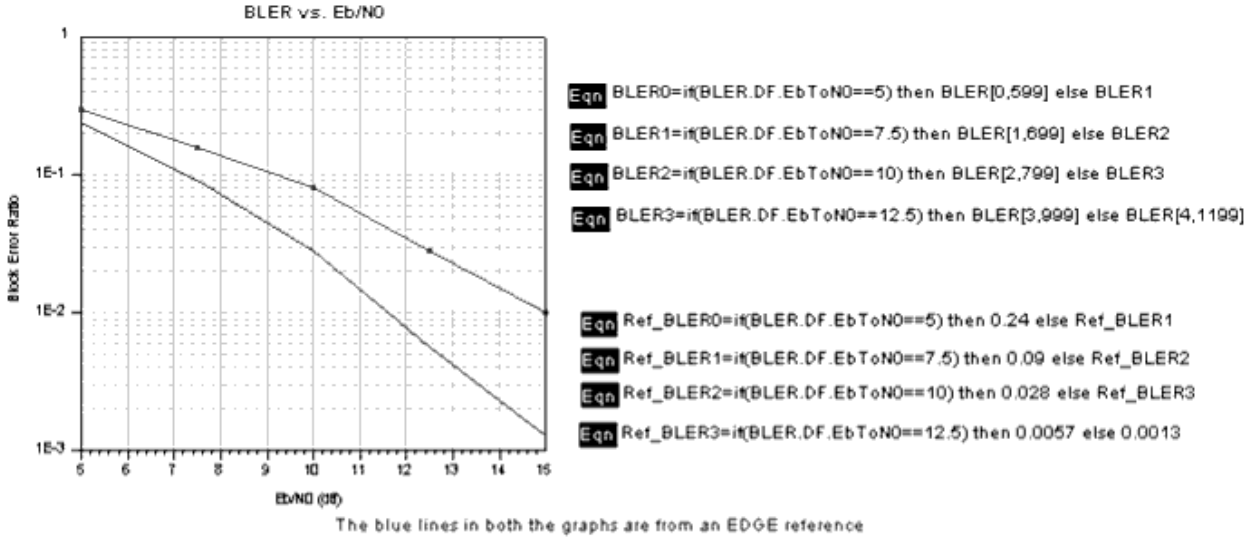
Symbol	Specification	Simulation Type	Value	Unit
SymbolRate	number of modulated symbols per second	Ptolemy	(1000.0×1625.0)/6	Hz
TSymbol	symbol interval	Ptolemy	1/SymbolRate	sec
FCarrier	carrier frequency	Ptolemy	935.2	MHz
TSC	training sequence code	Ptolemy	0	N/A
Ps	average power of received signal	Ptolemy	0.06826	W
EbToN0	Eb/N0 ratio	Ptolemy	5, 7.5, 10, 12.5, 15	dB

Notes

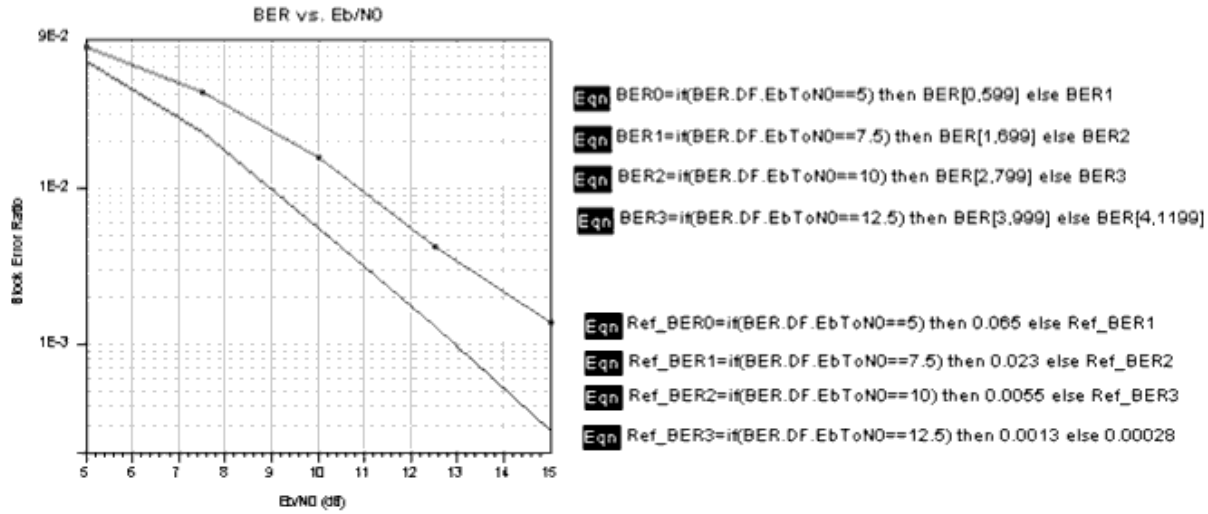
- SampleRate values of 4, 8 and 16 are supported
- TSC can be an integer from 0 to 7
- Ps must be the result of signal power measurement
- NoiseVar (in VAR) noise power value can be calculated using EbToN0 and Ps with an equation.

Simulation Results

The following figure shows the BER and BLER performance vs. Eb/N_0.



The blue lines in both the graphs are from an EDGE reference



The blue lines in both the graphs are from an EDGE reference

BER and BLER Performance vs. Eb/N_0

The following table lists the results of BER and BLER performance versus Eb/N_0.

Eb/N0 (dB)	BER	BLER
5	0.081	0.292
7.5	0.041	0.157
10	0.016	0.080
12.5	0.004	0.028
15	0.001	0.010

Benchmark

MCS1_DL_PwrMeasure

- Hardware platform: Pentium III 800 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 5000 bursts
- Simulation time: 16 minutes

MCS1_DL_HT100

- Hardware platform: Pentium III 450 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 10000 × 4 bursts
- Simulation time: 2.8 hours

Modulation and Coding Scheme 5 in Downlink

EDGE_MCS5_DL_wrk Design Names

- MCS5_DL_TU50
- MCS5_DL_PwrMeasure

Features

- GSM propagation fading channel and additive white Gaussian noise
- MCS-5 channel coding
- Channel interleaving and de-interleaving
- 8PSK modulation and RSSE equalization
- Gaussian noise with adjustable noise variance
- BER and BLER performance measured versus varies Eb/N0 ratio

Description

This example shows the system performance of BER and BLER (bit error rate and block error rate) for modulation and coding scheme 5 (MCS-5) in downlink. It consists of error correction coding and decoding, interleaving and de-interleaving, data framing and de-framing, 8PSK modulation, GSM fading channel (RF section) and additive white Gaussian noise, bit synchronization and an equalizer with reduced-state sequence estimation (RSSE) algorithm.

A random bit source is taken as user data source. Data is convolutionally coded at rate of 1/3, interleaved and fed into a normal burst construction component. After training, tail, and guard time bits are added, data is placed in an 8PSK modulation component. In this example only one user is considered.

The channel contains propagation fading and additive white Gaussian noise channels. Twelve channel types can be selected with adjustable parameters such as velocity, antenna height and location. In this example, the propagation fading channel is TU50-urban area and mobile station speed of 50 km/hr.

In the receiver, the signal is filtered by a 7-pole Butterworth filter (from the GSM Design Library). The bit synchronization component is used to determine the time delay and optimum downsample phase and perform delay adjustment and optimum downsampling. After signal recovery in the RSSE equalizer, burst disassembly, de-interleaving and channel decoding, BER and BLER are measured.

There are two designs in this example:

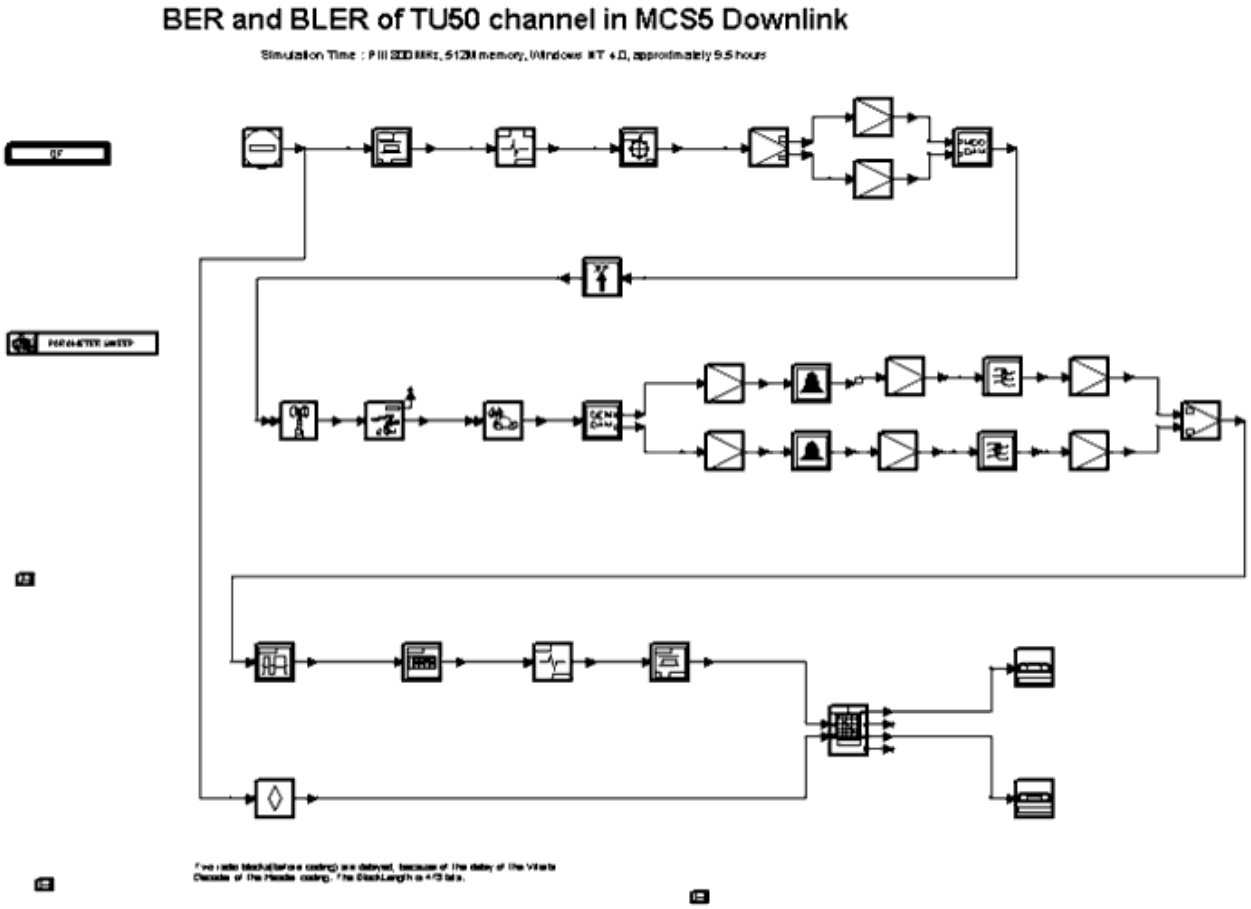
- MCS5_DL_PwrMeasure is used to measure the received signal power that will be used in calculating Eb/N_0 or SNR. EDGE_SigPowerMeasure outputs the average signal power once a burst. The guard symbols in bursts are not counted into the average power.
- MCS5_DL_TU50 is used to test BER and BLER over TU50 channel. The signal power is

entered into VAR2.Ps. When EbToN0 of VAR2, for Eb/N_0, is set the power of noise is automatically calculated by an equation. The value of Eb/N_0 is swept from 10 dB to 20 dB in 2 dB steps. EDGE_BERFER is used to measure BER and BLER. Because there is a delay of two blocks in channel decoding, the measurement starts from frame 2 and stops at frame 10002. A total of 10000 frames (10000 × 478 bits) are measured.

Schematics

The following figure shows the MCS1_DL_TU50 schematic. It contains random bit sources, normal burst construction, 8PSK modulation, RF section, fading channel, additive white Gaussian noise, bit synchronization, RSSE equalizer, normal burst disassembly and BER and BLER measurement.

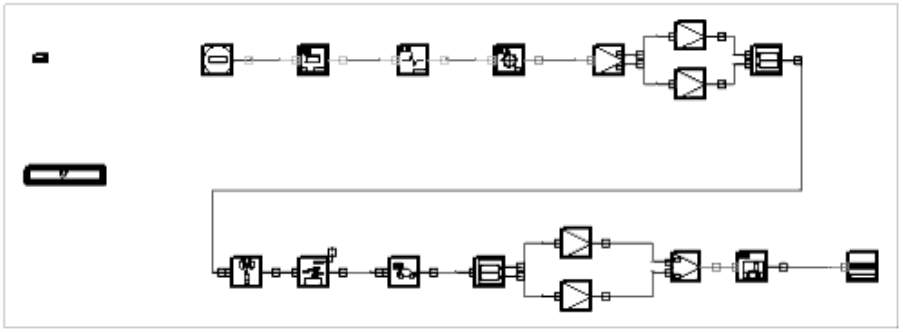
In the schematic, the disabled components are used for the average signal power measurement. The measurement is performed at the input of the receiver by EDGE_SigPowerMeasure. It outputs results once each burst.



MCS5_DL_TU50 Schematic

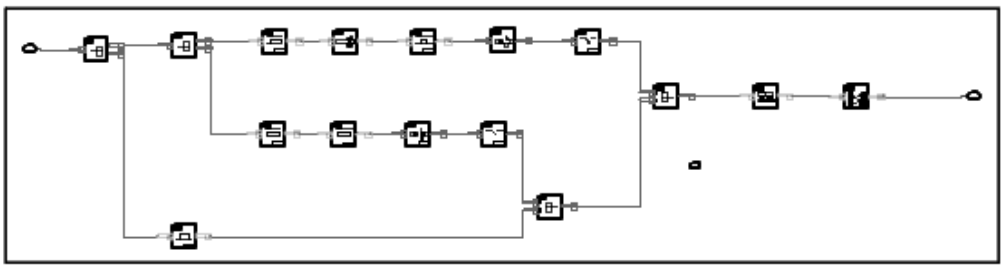
The following figure shows the MCS5_DL_PwrMeasure schematic. Compared to the design in the preceding figure, this design includes the transmitter, propagation fading channel and AWGN channel, a receiver component is not applied. The average signal power measurement is performed at the input of the receiver by EDGE_SigPowerMeasure. It

outputs results once each burst.



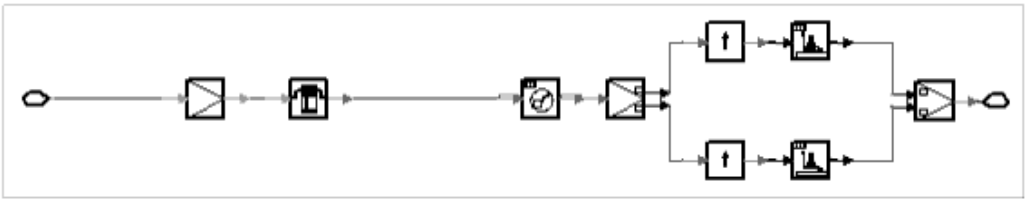
MCS5_DL_PwrMeasure Schematic

The following figure shows the EDGE_MCS5_DL_Encoder schematic. This subnetwork implements channel coding and channel interleaving of MCS-5 in downlink. In each input data block of 478 bits, there are three USF bits, 25 header bits and 450 data bits. The USF bits are pre-coded into 36 bits. Eight parity bits are added, convolutionally encoded with rate of 1/3, constraint length of 7, and punctured; the 25 header bits are encoded into 100 bits. The punctured header bits are interleaved by a header interleaver EDGE_HeaderIntrlv. Twelve parity bits are added to the 450-bit data block. By being convolutionally encoded and punctured, the 462-bit block results into a 1248-bit block. This 1248-bit data block is interleaved by EDGE_Interleaver. The encoded USF, header and data bits are combined into a 1384-bit block. After 8-bit coding scheme identifier is added, the data block has totally 1392 bits. These final 1392 bits are mapped into four bursts, and bits of each burst are swapped.



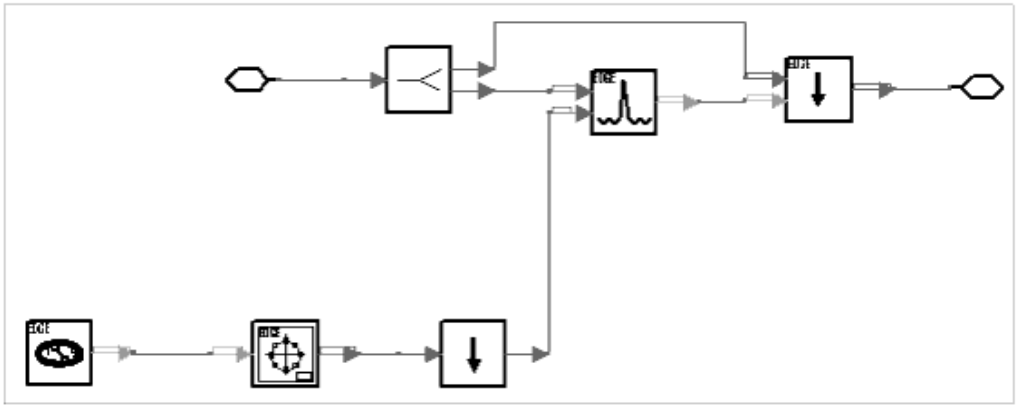
EDGE_MCS5_DL_Encoder Subnetwork Schematic

The following figure shows the 8PSK modulator EDGE_8PSKMod schematic. This subnetwork consists of Gray-mapping, phase rotation and pulse shaping. The phase rotation component performs the cumulative $\frac{3}{8}\pi$ phase rotation to the input symbols. The pulse-shaping filters are the linearized Gaussian filters as used in GMSK modulation.



EDGE_8PSKMod Subnetwork Schematic

The following figure shows the bit synchronization EDGE_BitSync schematic. This subnetwork consists of training sequence generation, 8PSK modulation, phase recovery and downsampler. The phase recovery component implements correlation calculation between the input signal and locally modulated training sequence to determine the time delay and the optimum downsampling phase. Using the output of phase recovery, the downsampler performs optimum downsampling and delay adjustment.

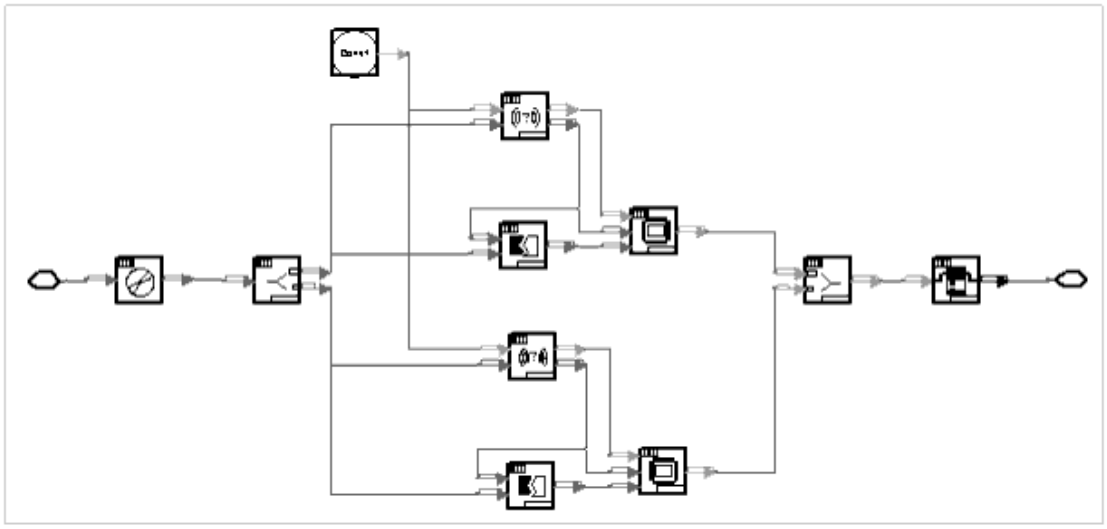


EDGE_BitSync Subnetwork Schematic

The following figure shows the adaptive equalizer EDGE_Equalizer schematic. This subnetwork implements the maximum likelihood sequence estimation (MLSE) algorithm for GMSK modulation and reduced-state sequence estimation (RSSE) algorithm for 8PSK modulation. It consists of de-rotation, burst splitting, channel estimation, matched filtering, Viterbi algorithm processor, burst combining and state-to-float converter.

The phase de-rotator is used the eliminate cumulative $\frac{3}{8}\pi$ phase rotation of 8PSK modulation or $\frac{\pi}{2}$ phase rotation introduced by differential encoding in GMSK modulation. The de-rotated burst is split into two sub-frames for the bidirectional equalization. Each sub-frame is matched filtered with the coefficient provided by channel estimator. The channel estimation is performed using the correlation characteristics of the training sequence.

The Viterbi algorithm processor is the core part of the equalizer. It implements the RSSE algorithm by using Ungerboeck state partition method and a modified Viterbi algorithm and the MLSE algorithm. It gives out the hard decided results of state numbers of the 8PSK or BPSK modulation. The state numbers are finally translated into bits by the state-to-float converter.



EDGE_Equalizer Subnetwork Schematic

The following figure shows the MCS-5 downlink channel decoding EDGE_MCS5_DL_Decoder schematic. This subnetwork implements the inverse process of the channel coding component EDGE_MCS5_DL_Encoder. It consists of bit de-swapping, burst de-mapping, de-interleaving, de-puncturing, Viterbi decoder and cyclic code decoder. Because there is a delay of five times the constraint length introduced by EDGE_ViterbiBitDCC, some extra delays are needed. The final output of the channel decoder has a delay of two blocks, i.e. 478 × 2 = 956 bits.

EDGE_MCS5_DL_Decoder Subnetwork Schematic

Symbol	Specification	Simulation Type	Value	Unit
SymbolRate	number of modulated symbols per second	Ptolemy	(1000.0×1625.0)/6	Hz
TSymbol	symbol interval	Ptolemy	1/SymbolRate	sec
FCarrier	carrier frequency	Ptolemy	935.2	MHz
TSC	training sequence code	Ptolemy	0	
Ps	average power of received signal	Ptolemy	1.6693	W
EbToN0	Eb/N0 ratio	Ptolemy	5, 7.5, 10, 12.5, 15	dB

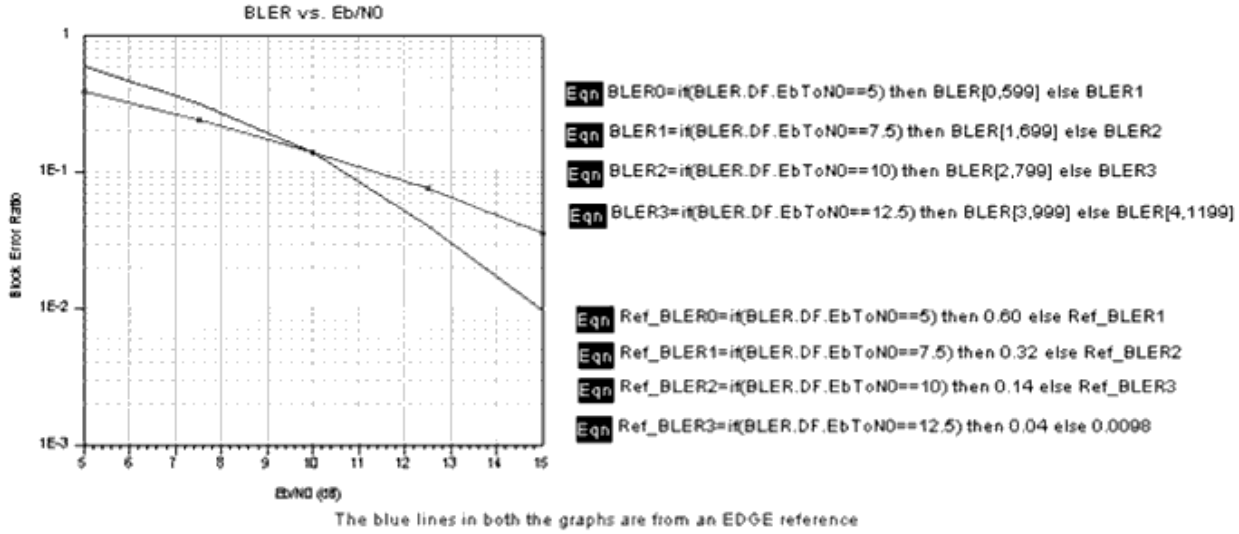
Notes

- SampleRate must be a integer > 0.

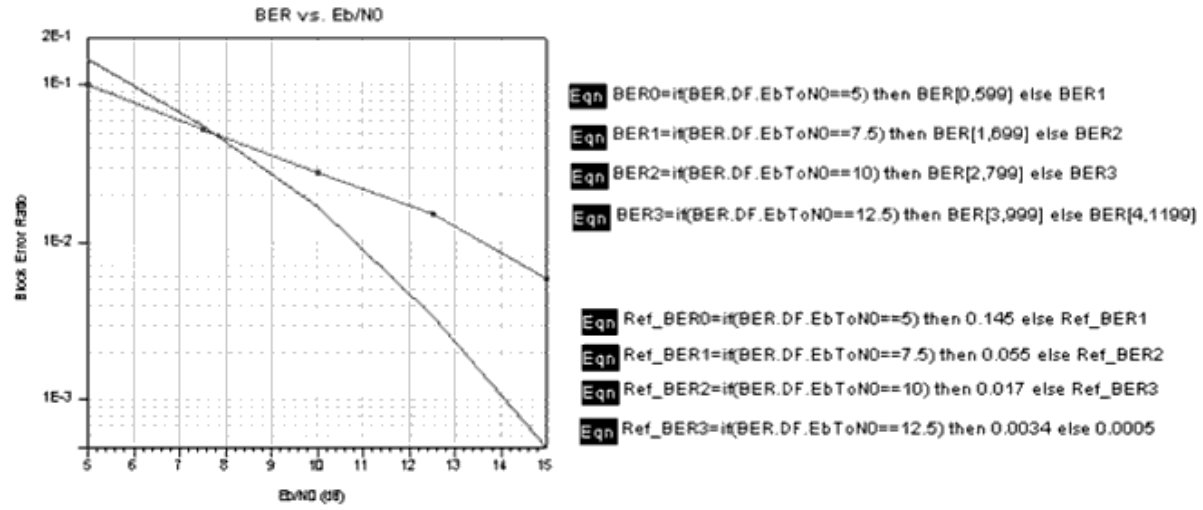
- TSC can be a integer from 0 to 7.
- Ps must be the result of signal power measurement.
- NoiseVar (in VAR) noise power value can be calculated using EbToN0 and Ps with an equation.

Simulation Results

The following figure shows the BER and BLER performance vs. Eb/N0.



The blue lines in both the graphs are from an EDGE reference



The blue lines in both the graphs are from an EDGE reference

BER and BLER Performance vs. Eb/N0

The following table shows the numeric results of BER and BLER performance versus Eb/N0.

Eb/N0 (dB)	BLER	BER
5	0.387	0.1
7.5	0.239	0.052
10	0.139	0.028
12.5	0.077	0.015
15	0.036	0.006

Benchmark: MCS5_DL_PwrMeasure

- Hardware platform: Pentium III 800 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 2000 bursts
- Simulation time: 40 minutes

Benchmark: MCS5_DL_TU50

- Hardware platform: Pentium III 800 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 10000 × 4 bursts
- Simulation time: 9.5 hours

EDGE Traffic Channel Measurement in RF

EDGE_RF_Measurement_wrk Design Names

- EDGE_Ideal_System
- EDGE_RF_Section

Features

- 8PSK modulation with pulse shaping filter and continuous $\frac{3}{8}\pi$ symbol phase rotation
- framed user data
- simulate mixed GSM and EDGE time slots
- optional alternate time slot power level control
- adjustable sample rate
- integrated RF section
- co-simulation of DSP and analog/RF components
- spectrum analysis and EVM measurements

Description

This example demonstrates the EDGE transmission; it includes normal burst construction, framing, 8PSK and GMSK modulation, and RF section. Error vector magnitude (EVM) is measured. Spectrum analysis is performed at the output of the RF section. Results of all these measurements comply to the measurement results of instruments.

This example includes GSM users (data is modulated in GMSK), and EDGE users (data is 8PSK modulated). Normal bursts for each user are built according to the GSM burst structure. The number of bits in bursts of EDGE users is three times that in GSM bursts. In framing, each bit in bursts of GSM users is repeated three times to make the bursts of all users have same length. Using the normal burst construction component, the modulation type, training sequence code (TSC) and tail bits can be set by designers. The stealing flag bits are input from pin SF. The training sequences used are the same as those defined in GSM 05.02, except in burst of EDGE users the training sequence is transformed from 26 bits into 78 bits by mapping 0 into 001 and 1 into 111.

The framed data is modulated by a GMSK modulator and an 8PSK modulator. For a GSM user, each three bits (the repeated bits) are cut into one bit before GMSK modulation. By using a Mux component controlled by a WaveForm component, a modulated frame with mixed GSM and EDGE time slots is generated. The power of each time slot is controlled separately by a WaveForm component.

Modified 8PSK modulation, a key features of EDGE, is included in this example. 8PSK is a linear modulation, where three consecutive bits are Gray-mapped into one symbol on the I/Q axis, with a symbol rate of 270.833 kilosymbols per second. To avoid the envelope of modulated signals becoming zero, symbols are rotated by $\frac{3}{8}\pi$ radians per symbol, the

constellation is rotated and does not go through the origin. A sequence of complex exponential symbols is generated by the phase generation section to implement continuous $\frac{3}{8}\pi$ phase rotation.

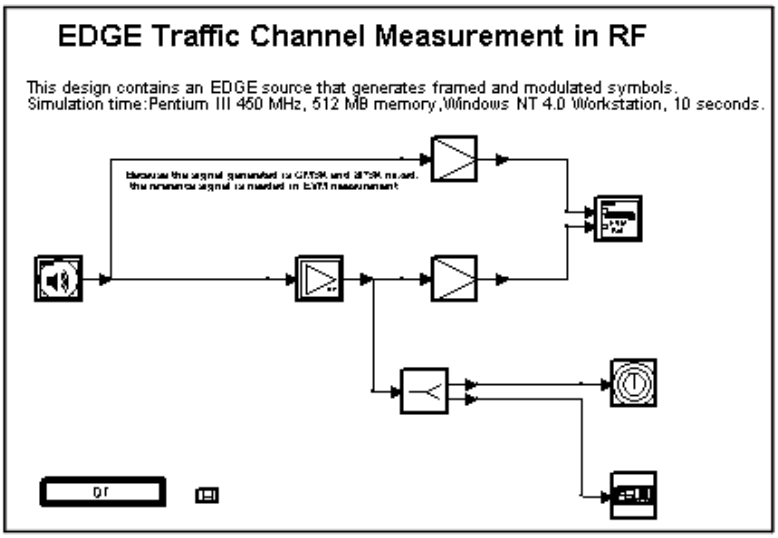
A pulse-shaping filter is used to minimize the impact on the spectrum, especially for the adjacent channels. This filter is equivalent to the main component in the Laurant expansion of GMSK modulation (the Laurant expansion provides a method for expressing binary CPM signals as a sum of amplitude modulated pulses), its impulse response is *C* 0(*t*).

The EDGE_Source subnetwork is used to generate the framed multi-user signal. It also converts the signal from baseband to RF. In EDGE_Ideal_System, the RF signal is fed into an ideal RF power amplifier. EVM and spectrum measurements are performed at the output of the amplifier. Similarly, in EDGE_RF_Section, a transmission chain subnetwork that contains filters, amplifiers and mixer is used instead of an ideal RF amplifier.

Envelopes of symbols throughout eight time slots are recorded in a sink.

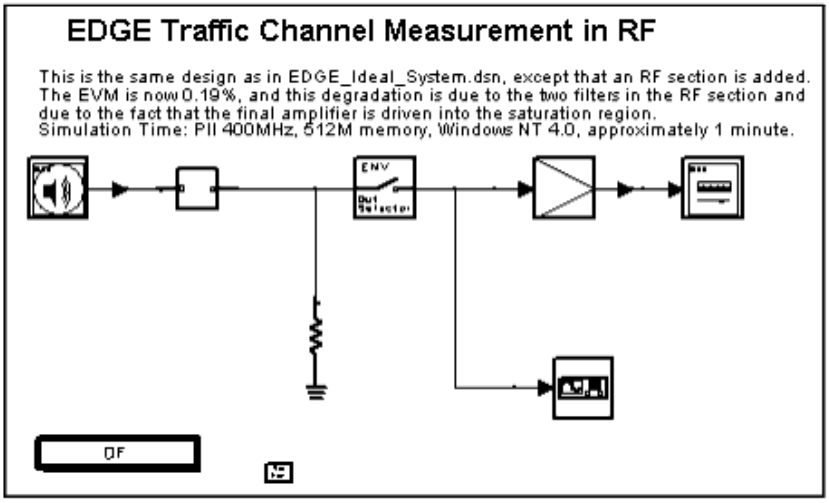
Schematics

The following figure shows the EDGE_Ideal_System schematic. It contains EDGE RF source generation, RF amplifier, spectrum analyzer, EVM measurement and a sink.



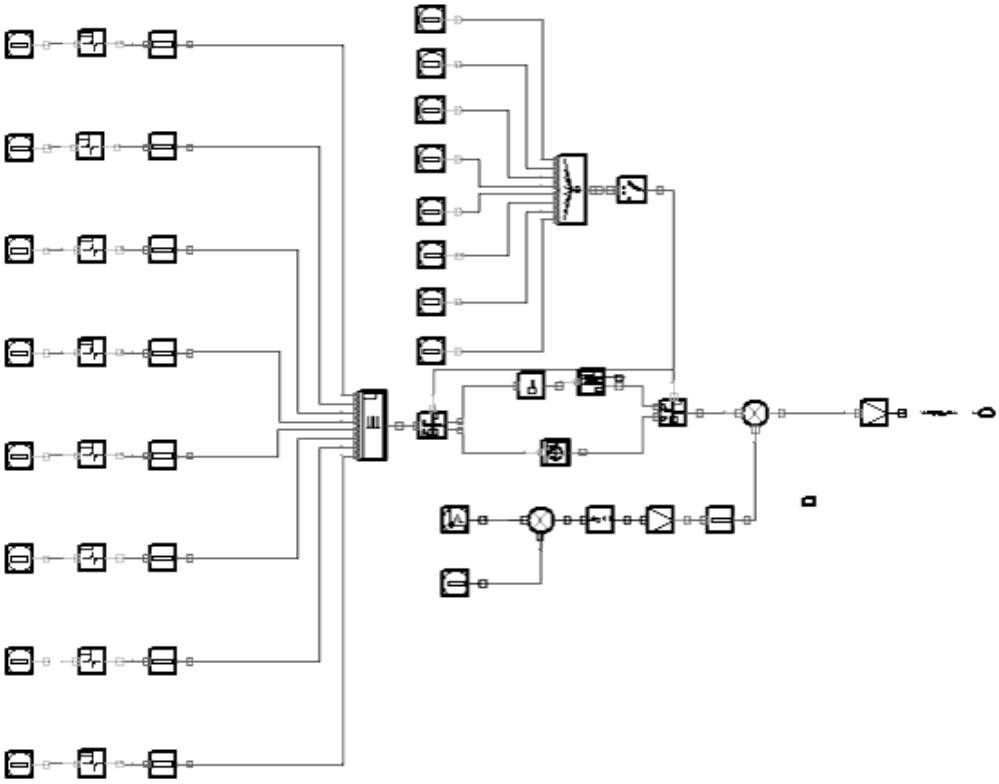
EDGE_Ideal_System Schematic

The following figure shows the EDGE_RF_Section schematic. In contains a transmission chain subnetwork.



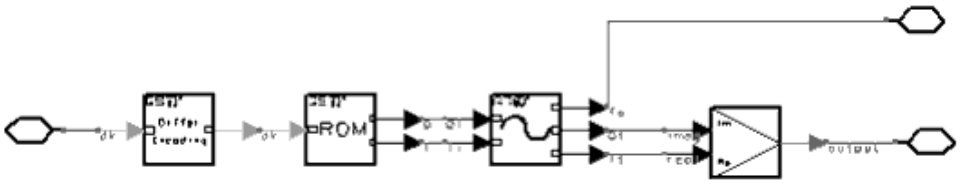
EDGE_RF_Section Schematic

The following figure shows the EDGE_Source subnetwork.



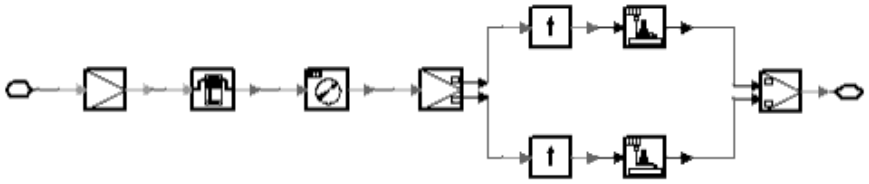
EDGE_Source Subnetwork Schematic

The following figure shows the structure of EDGE_GMSKMod used in EDGE_Source. It consists of EDGE_DifferEncoder, EDGE_Rom and EDGE_Carrier.



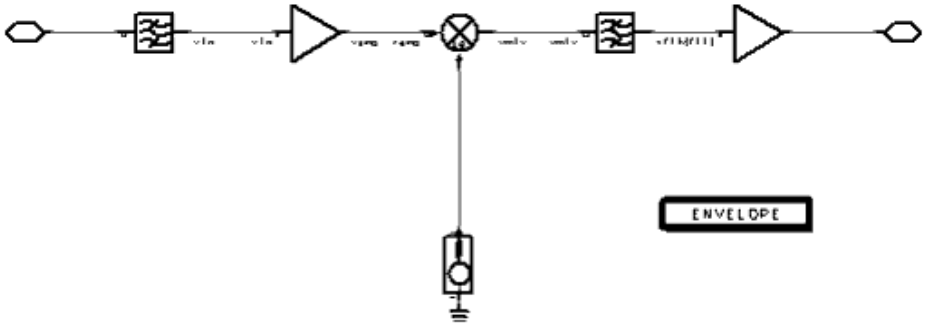
EDGE_GMSKMod Schematic

The following figure shows the modified 8PSK modulation in EDGE_Source. It consists of Gray-mapping section, phase rotation section and pulse shaping filter.



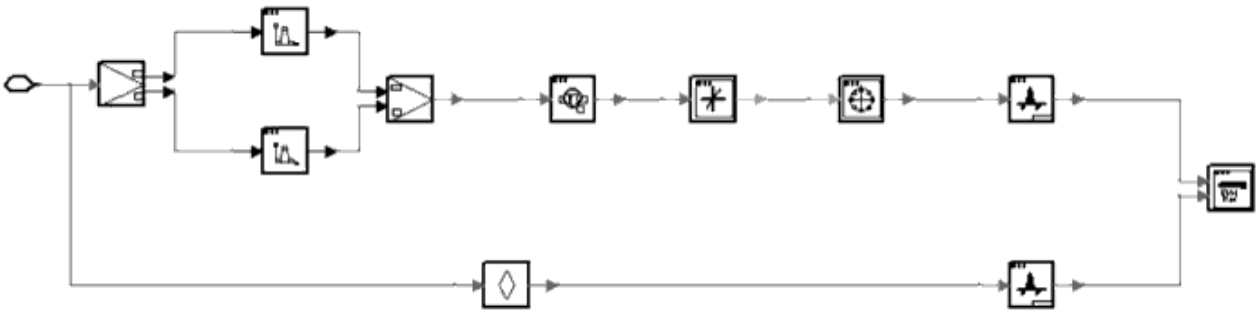
Modified 8PSK Modulation Schematic

The following figure shows the structure of transmission chain TXchain. It contains bandpass filters, amplifiers, local oscillator and mixer.



TXchain Schematic

The following figure shows the structure of EDGE_EVM used to perform the 8PSK modulated signal EVM measurement in this example. In this subnetwork, receiver filters are used to eliminate the inter-symbol interference (ISI) introduced by the pulse shaping filters in 8PSK modulation.



EDGE_EVM Subnetwork Schematic

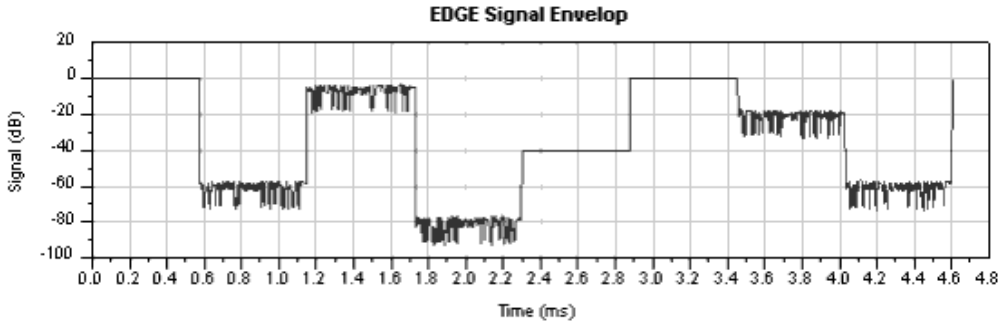
Symbol	Specification	Simulation Type	Value
UpSample	number of samples in one symbol	Ptolemy	8
SampPerSym	enumerated type of UpSample	Ptolemy	int(UpSample/8)
TSymbol	time duration of symbols	Ptolemy	1/(1000×1625/6)
TSample	time duration of samples	Ptolemy	TSymbol/UpSample
BurstLength	length of a burst on which EVM measurement is performed	Ptolemy	156×TSymbol

Notes

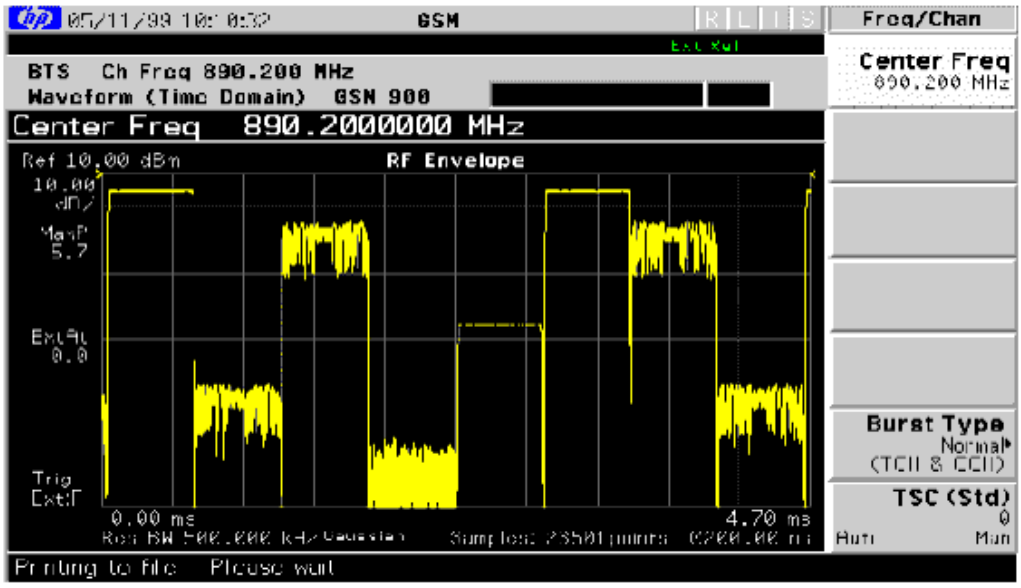
- Sample rates supported are UpSample = 4, 8, 16; the corresponding SampPerSym is 0, 1, 2.

Simulation Results

- Symbol Envelope
  The following figure shows the symbol envelopes throughout a EDGE frame with mixed GSM and EDGE time slots.



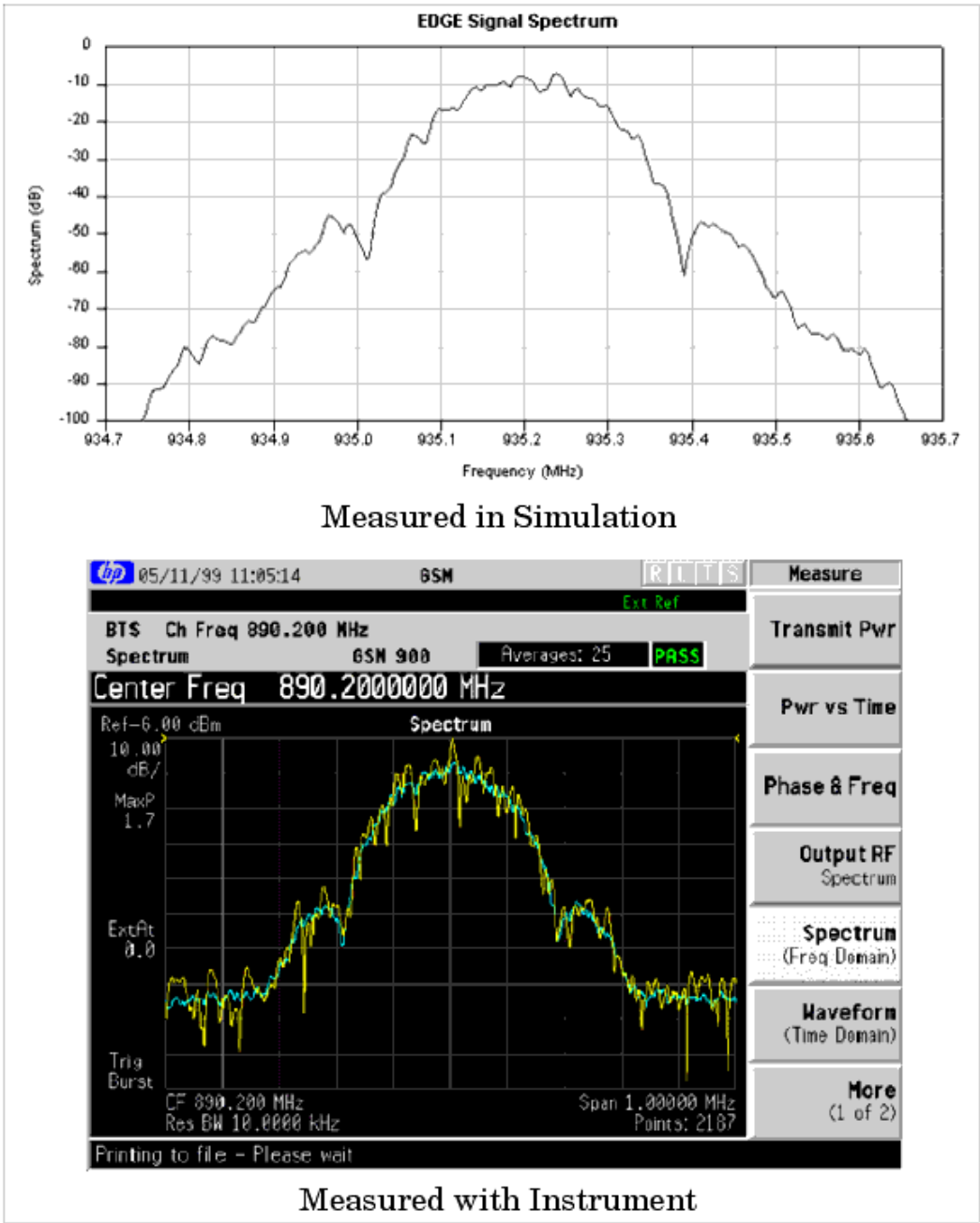
Symbol Envelopes Recorded in Simulation



Symbol Envelopes Measured with Instrument

Symbol Envelopes Throughout EDGE Frame

- Spectrum of 8PSK Modulation
  The following figure shows the spectrum of 8PSK modulation.



Spectrum Analysis of 8PSK Modulation

- Error Vector Magnitude (EVM)
  The value of EVM for the ideal RF amplifier is 4.690e-17.
  The value of the transmission chain is 0.0016. Because of the non-linearity of filters and mixer in the chain, the EVM value is greater than that of the ideal RF amplifier.

Benchmark

- Hardware platform: Pentium III 450 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 8 × 156 × SampleRate
- Simulation time:
  10 seconds for EDGE_Ideal_System;

1 minute for EDGE_RF_Section

Error Vector Magnitude Measurement Examples

EVM_Examples_wrk Design Names

- EVM_SAWFilter_2Pin
- EVM_SAWFilter_1Pin
- EVM_NonLinearAmp
- SAWFilter_Character

Features

- EVM measurement for a SAW filter (GSM/EDGE channel selective filter) using 1-pin and 2-pin EVM models
- EVM measurement for non-linear amplifier using the 2-pin EVM model
- RMS EVM, peak EVM, and 95th percentile measured
- standard EDGE 8PSK modulation
- Circuit envelope co-simulation for SAW filter
- S-parameter simulation of SAW filter
- EDGE measurement filter (raised-cosine-windowed-raised-cosine filter)

Description

This workspace demonstrates the use of 1- and 2-pin EVM models for EVM measurements. A comparison of the results of these EVM models is provided. Two components are tested as examples: the SAW (surface acoustic wave) filter, which is similar to the GSM/EDGE channel selective filter, and the non-linear amplifier.

The four designs in this workspace also demonstrate how to use the SAW filter by using co-simulation and how to measure its characters.

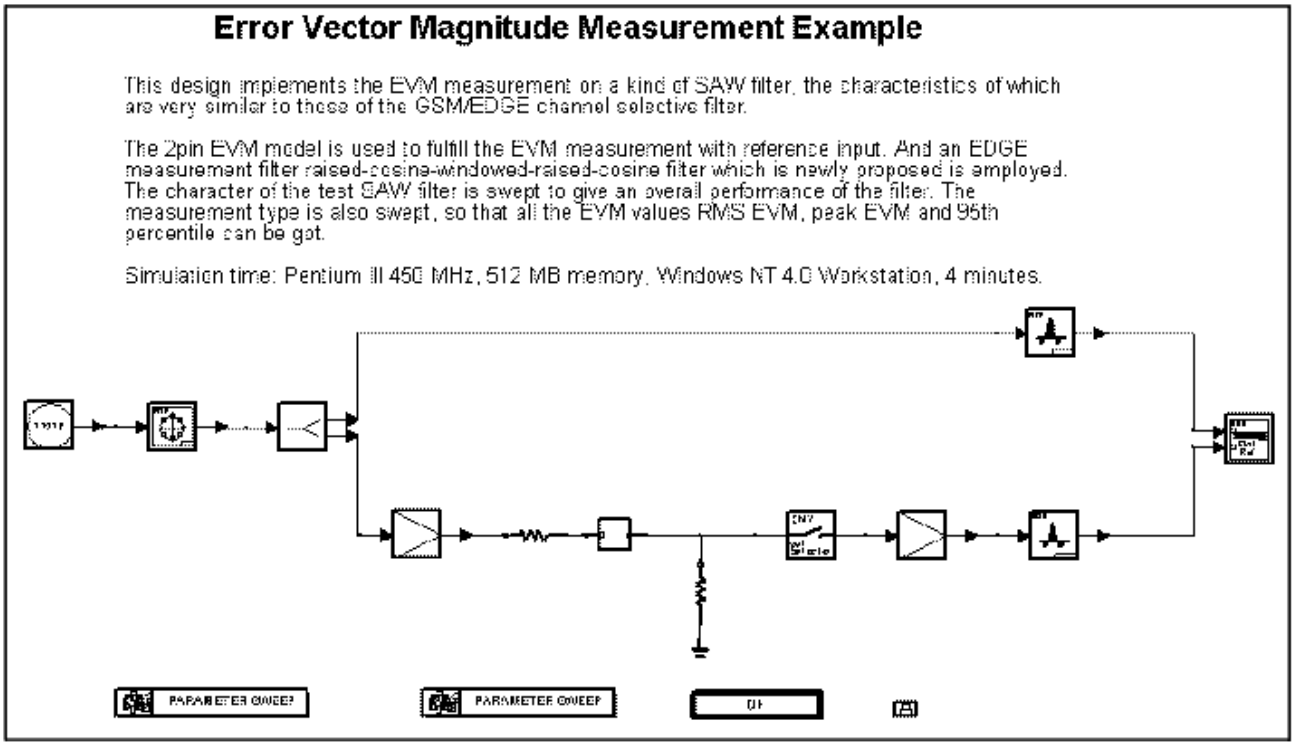
EVM_SAWFilter_2Pin uses the 2-path scheme that requires reference signal input. EVM_SAWFilter_1Pin uses the single-path scheme in which the original signals are automatically retrieved inside the EDGE_EVM subnetwork and reference signal are not needed.

The EVM measurements include RMS EVM, peak EVM and 95th percentile, which are according to the latest EDGE specifications. Results of the two EVM schemes are compared in the data display file EVMResults.dds.

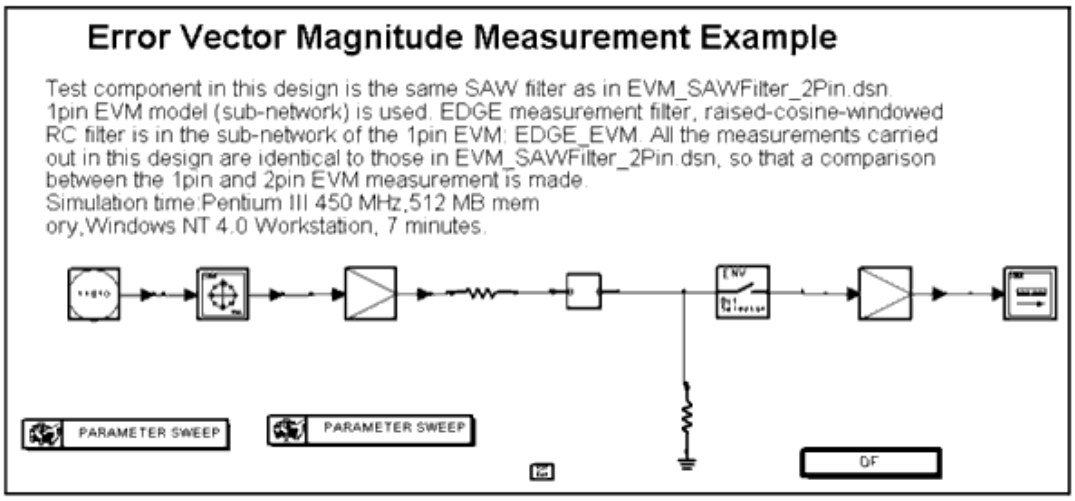
Schematics

The first of the following two figures is the EVM_SAWFilter_2Pin schematic; the second is the EVM_SAWFilter_1Pin schematic. In the first figure, at the left are the source and 8PSK modulation. Signals are split into the reference (upper) path and the test path. The SAW filter (regarded as the GSM/EDGE channel selective filter) for the EVM measurement, EDGE_SAWFilter subnetwork, is in the test path. An EnvOutSelector is used for co-

simulation. The design sweeps parameter Aripple, which represents the amplitude variation of the SAW filter from 0.0 dB to 3.5 dB in steps of 0.5 dB, to show the influence of performance variation of the filter on the EVM value. It also sweeps the MeasType (measurement type), from EVM_rms to EVM_95th_percentile.

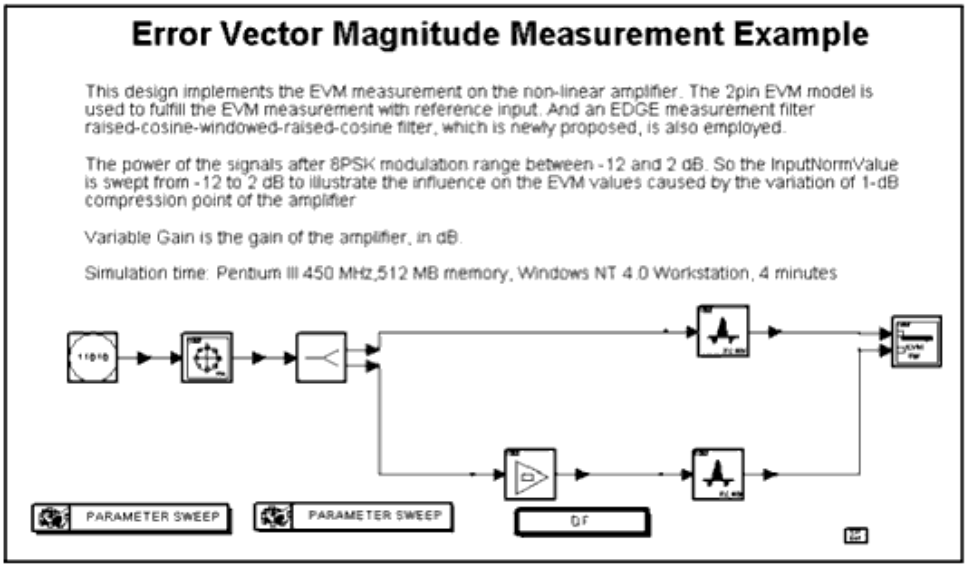


EVM_SAWFilter_2Pin Schematic



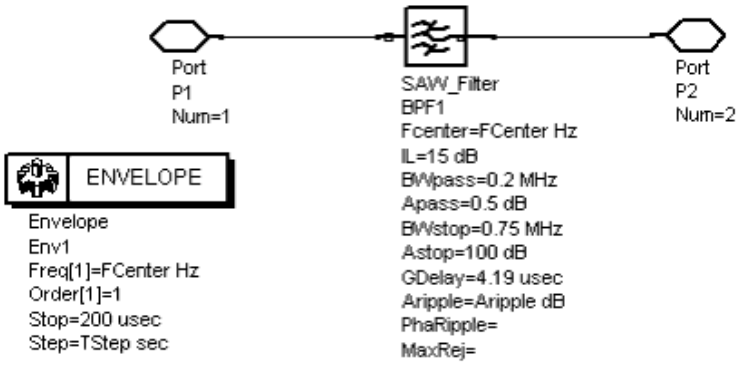
EVM_SAWFilter_1Pin Schematic

EVM_NonLinearAmp, the following figure, implements the EVM measurement on the non-linear amplifier using the 2-path EVM scheme. The 1-dB compression point of the amplifier is the key parameter in this measurement and it is swept in the design. The measurement type is also swept. Results are saved in EVMResults.dds.



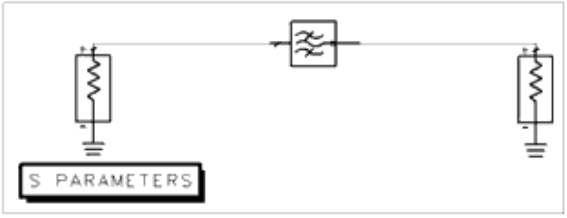
EVM_NonLinearAmp Schematic

The following figure shows the SAW filter subnetwork (GSM/EDGE channel selective filter) used in the EVM measurement for envelope simulation.



EDGE_SAW_Filter Schematic

SAWFilter_Character, the following figure, is an S-parameter simulation design. It can be used to measure and calculate the S-parameters of the SAW filter. Results are saved in SAWFilter_Character.dds.



SAWFilter_Character Schematic

Specifications

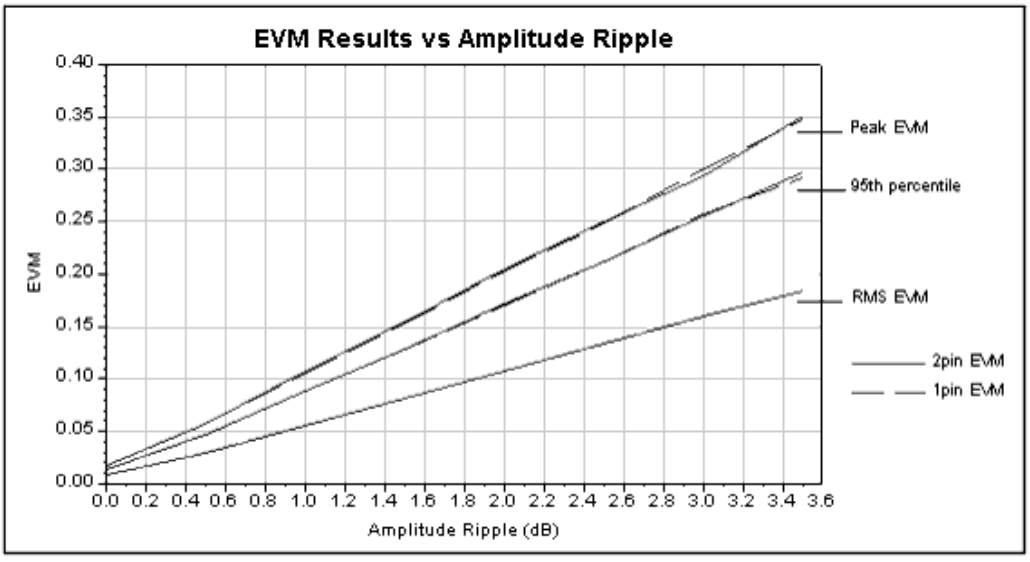
Symbol	Specification	Simulation Type	Value
StartSym	start symbol for EVM measurement	Ptolemy	142 †
SymBurstLen	number of symbols within burst to be measured for EVM	Ptolemy	142
SampPerSym	number of samples per symbol	Ptolemy	16
NumBursts	number of bursts to be measured for EVM	Ptolemy	5
Aripple	passband amplitude ripple, in dB	Circuit Envelope & S-parameter	0.0 to 3.5
InputNormValue	input normalization value, in dBw	Ptolemy	-12 to 2
OutputNormValue	out normalization value, in dBw	Ptolemy	InputNormValue+ 3dB

† Set StartSym to142, the length of the useful part of EDGE normal burst, in order to measure EVM from the beginning of the second burst. †† InputNormValue (dBw), OutputNormValue (dBw) is the 1dB compression point of the non-linear amplifier. Normalizing according to these two parameters makes the (0,0) point in the output character figure correspond to the 1dB compression point.

Simulation Results

The following figure shows the simulation results of the EVM measurement on the SAW filter. Solid lines represent the values (RMS EVM, peak EVM and 95th percentile) obtained from 2-pin model; dashed lines represent the values from 1-pin model. Curves correspond to different amplitude ripples (variations) of the SAW filter. The group delay ripple varies when the amplitude ripple varies; the following table lists amplitude and group delay ripples of this filter.

Results in the figure are similar to those in EDGE. And it can be seen that the 1- and 2-pin EVM models are consistent with each other.

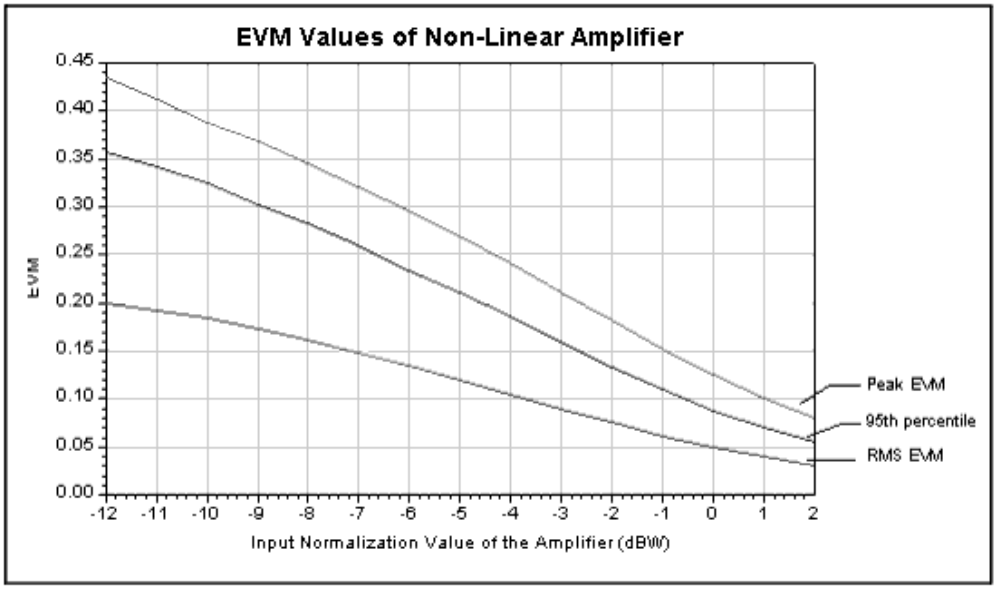


EVM Results of the Sweep of Amplitude Variation of the SAW Filter

Amplitude Ripple (dB)	Group Delay Ripple (µsec)
0.0	0.0
0.5	0.25
1.0	0.50
1.5	0.75
2.0	1.00
2.5	1.25
3.0	1.50

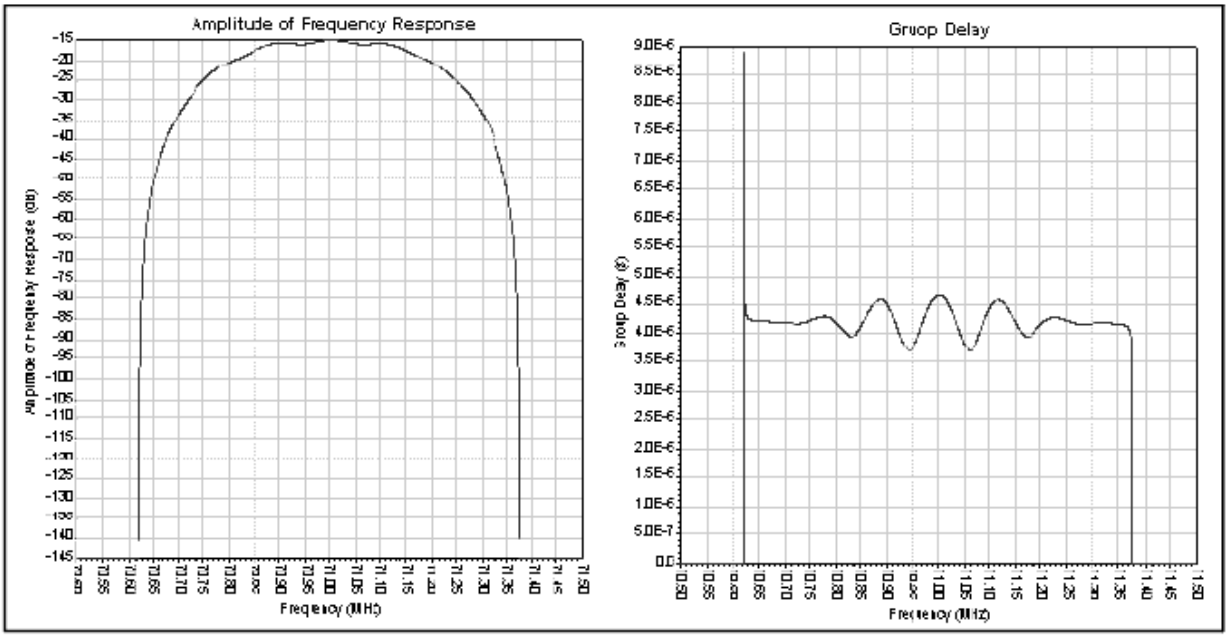
The following figure shows the result of EVM measurement on the non-linear amplifier. X-coordinate is the input normalization value; the Y-coordinate is the EVM value. The curves represent the RMS EVM, peak EVM and 95th percentile. The power of the signals after 8PSK modulation range between -12 and 2 dB. So the InputNormValue is swept from -12 to 2 dB to illustrate the influence on the EVM values caused by the variation of 1-dB compression point.

It is clear that the EVM value decreases when the input normalization value increases. The reason is that when the input normalization value increases, more of the input signal power falls into the linear zone of the amplifier, causing less signal distortion.



RMS EVM, Peak EVM, 95th percentile vs. Input Normalization Value (dB) of Non-Linear Amplifier

The following figure shows the results of the S-parameter simulation on the SAW filter with 1dB amplitude variation (ripple). The plots show clearly the width and shape of the passband and the shape of the group delay ripple. It can be seen that the group delay variation corresponding to 1 dB amplitude ripple is approximately 0.5 µsec.



Amplitude (left) and Group Delay (right) of the SAW Filter Frequency Response (amplitude ripple = 1.0 dB)

Benchmark: EVM_SAWFilter_2Pin

- Hardware platform: Pentium III 450 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 6 × (142 + 3) × 16 × 8 × 3 = 334080
- Simulation time: 4 minutes

Benchmark: EVM_SAWFilter_1Pin

- Hardware platform: Pentium III 450 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 6 × (142 + 3) × 16 × 8 × 3 = 334080
- Simulation time: 7 minutes

Benchmark: EVM_NonLinearAmp

- Hardware platform: Pentium III 450 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 6 × (142 + 3) × 16 × 15 × 3 = 626400
- Simulation time: 4 minutes

EDGE Mobile Station Receiver Design Examples

Introduction

The MS_RX_wrk workspace provides design examples of mobile station receiver measurements including minimum input performance levels, co-channel rejection, adjacent channel rejection, and blocking characteristics. Measurements are based on 14.18 of GSM 11.10 and corresponding EDGE *Change Request* documents.

Designs for these measurements include:

- Minimum input performance levels under static and multipath conditions: MS_RxSRSL, MS_RxMRSL
- Co-channel rejection: MS_RxCoCH_Rejection
- Adjacent channel rejection: MS_RxAdCH_Rejection
- Blocking characteristics: MS_RxBlocking_Test

Designs in this workspace consist of:

- BTS signal source in baseband
  EDGE_BTS_MCSN_PwrCtrlSrc (N = 5, ... , 9) generates the downlink encoded, framed and modulated baseband signal. The power level of each time slot of the signal can also be controlled with this source.
- Transmission modulation and up-converter
  Data from EDGE_BTS_MCSN_PwrCtrlSrc is up-converted to a 71 MHz IF signal with EDGE_RF_Mod, then modulated into a 935 MHz RF signal with EDGE_RF_TX_IFin.
- Channel loss and interfering signal combination
  The transmitted RF signal is then attenuated by RF channel (GainRF model) and combined with interfering signals (modulated or continuous waveform) at given frequency offsets. Propagation conditions are also simulated in some designs.
- Down-converter and demodulation
  At the receiver side, the received signal is demodulated to be the baseband signal by EDGE_RF_RX_IFout and EDGE_RF_Demod.
- Mobile station receiver in baseband
  EDGE_MS_MCSN_Receiver, where N = 5, ... , 9, is used to demodulate and decode the received baseband signal.

Minimum Input Level Performance, Static Conditions

MS_RxSRSL

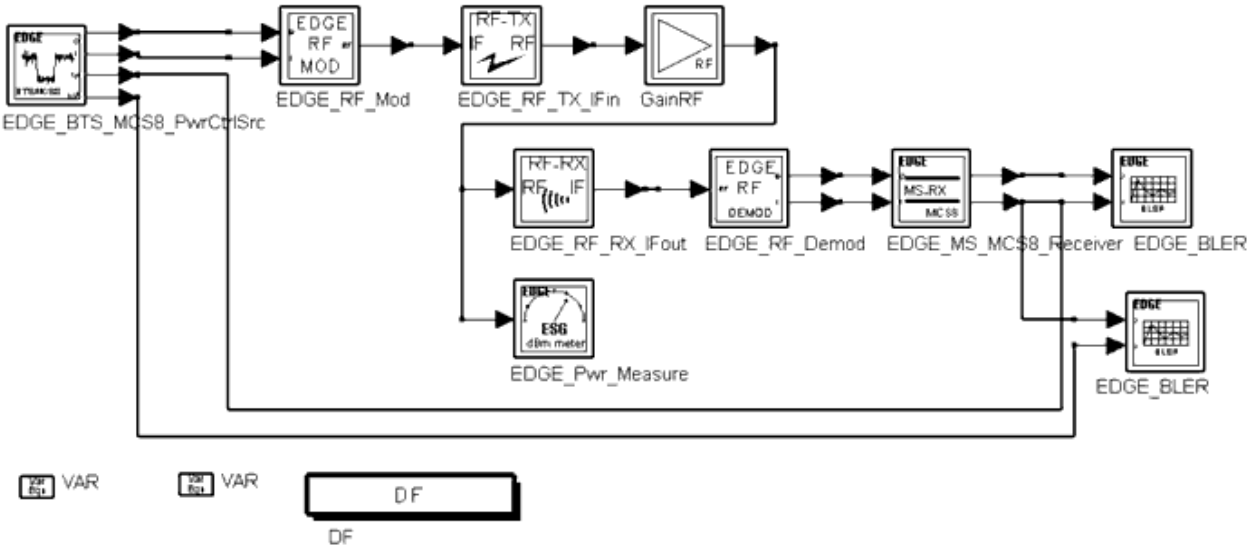
Features

- minimum input performance levels under static conditions
- BLER of PDTCH and BER of USF measurements

Description

The base station transmits packets on the allocated time slot to the mobile station under static propagation conditions, using MCS8 coding. On time slots not allocated to the mobile station, the base station transmits data at a power level 20dB above that of the allocated time slot. This implicitly tests adjacent time slot rejection.

Schematic



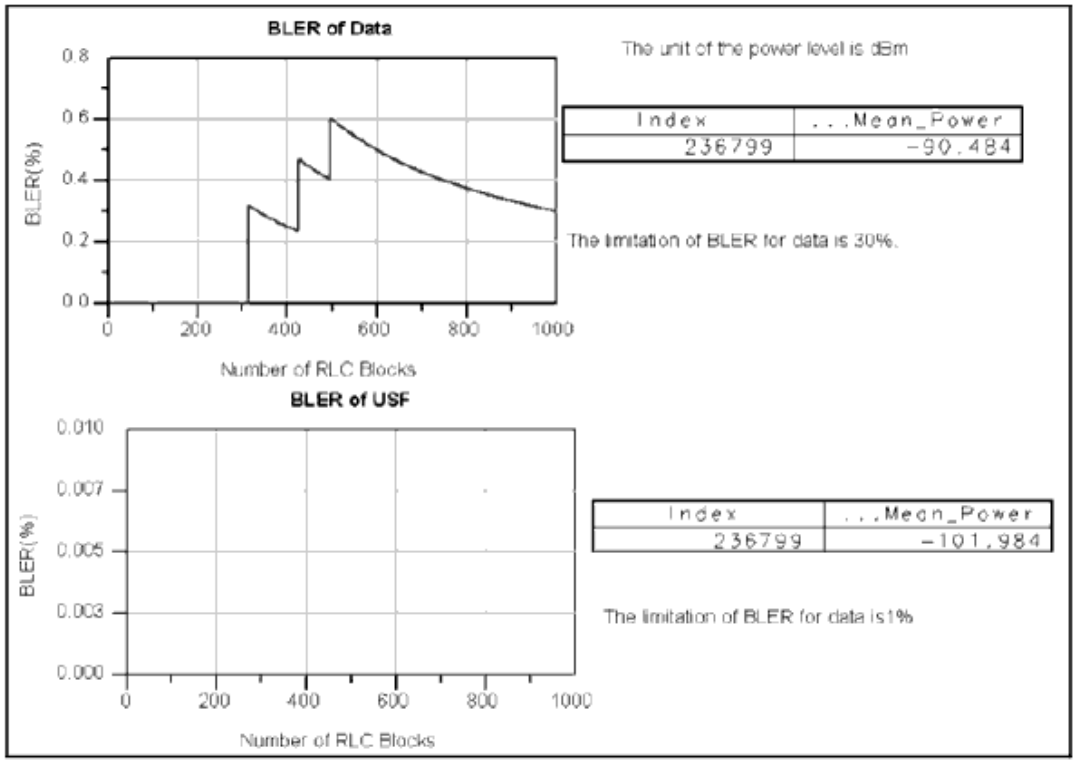
MS_RxSRSL Schematic

Notes

When the block error rate (BLER) performance for PDTCH is simulated, Ps is set to 90.5 and PDTCH_BLER is activated while USF_BLER is de-activated. When the BLER performance for USF is simulated, Ps is set to −102 and PDTCH_BLER is de-activated while USF_BLER is activated.

Test Results

Test results displayed in the MS_RxSRSL.dds file are shown in the following figure.



Data and USF BLER

Benchmark

- Hardware platform: Pentium II 400 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Data Points: 1000 blocks.
- Simulation time: approximately 10 hours

Minimum Input Level Performance, Multipath Conditions

MS_RxMRSL

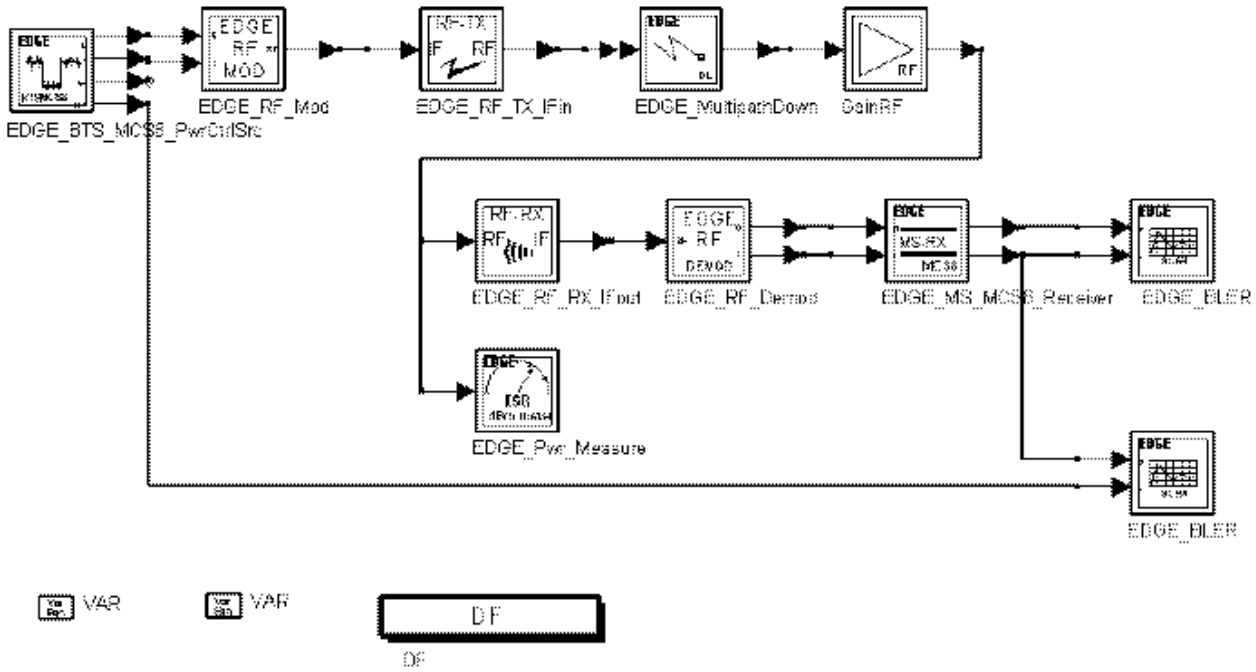
Features

- minimum input performance levels under multipath conditions
- BLER of PDTCH and BER of USF measurements

Description

The base station transmits packets on the allocated time slot to the mobile station under multipath propagation conditions using MCS8 coding. On time slots not allocated to the mobile station, the base station does not transmits data.

Schematic



MS_RxMRSL Schematic

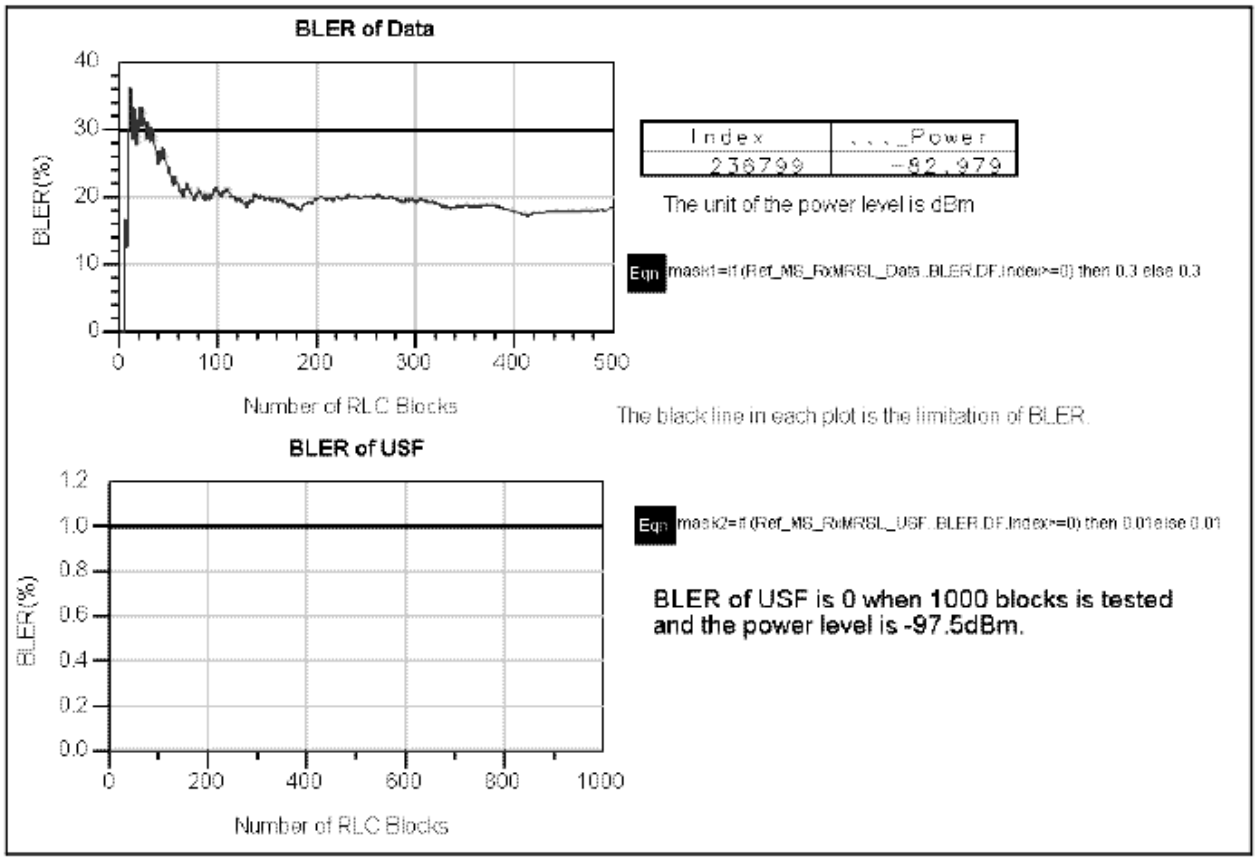
Notes

When the block error rate (BLER) performance for PDTCH is simulated, Ps is set to 83 and PDTCH_BLER is activated while USF_BLER is de-activated. When the BLER performance for USF is simulated, Ps is set to −97.5 and PDTCH_BLER is de-activated while USF_BLER

is activated.

Test Results

Test results displayed in the MS_RxMRSL.dds file are shown in the following figure.



BLER of Data and USF

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, ADS 1.3
- Data Points: 500 blocks
- Simulation Time: approximately 6 hours

Co-Channel Rejection Measurements

MS_RxCoCH_Rejection

Features

- co-channel rejection of data and USF of PDTCH downlink measurements
- integrated RF section
- GMSK modulated continuous interference signal (I1)
- C/Ic measured and calibrated
- propagation model

Description

This design demonstrates how to test the co-channel rejection of EGPRS mobile station receiver. The test is based on specifications and requirements in 14.18.2 of GSM 11.10 and corresponding EDGE *Change Request* documents.

Co-channel rejection is a measure of the receiver's ability to receive a modulated signal without exceeding a given degradation due to the presence of an unwanted modulated signal, both signals being at the nominal frequency of the receiver. The signal wanted in this test is the signal generated by the transmitted RLC data blocks.

The BTS transmits packets on PDTCH using MCS5 coding to the mobile station on the allocated time slot (TS_Measured). On all other time slots, no signal is transmitted. The co-channel interference ratio is set 1 dB above the ratio given in the following table.

MCS5 is used in this design example. Tests for MCS5, ... , MCS9 can be performed using EDGE Design Library models EDGE_BTS_MCSN_PwrCtrlSrc and EDGE_MS_MCSN_Receiver.

Co-channel Interference Ratio for 8PSK Modulation

GSM 400 and GSM 900				
Type of Channel	**Propagation Conditions**			
	TUlow (no FH)	**TUhigh (no FH)**	**TUhigh (ideal FH)**	**RA(no FH)**
PDTCH MCS-5 (dB)	19.5	15.5	14.5	16.5
PDTCH MCS-6 (dB)	21.5	18	17.5	21
PDTCH MCS-7 (dB)	26.5	25	24.5	†
PDTCH MCS-8 (dB)	30.5	25.5 ††	25.5 ††	†
PDTCH MCS-9 (dB)	25.5 ††	30.5 ††	30.5 ††	†
† Does not meet reference performance. †† Performance is specified at 30% BLER.				

Test requirements are:

- The block error rate (BLER) performance for PDTCH/MCS5 to 9 not to exceed 10% or 30% depending on coding schemes at co-channel interference ratios (C/Ic) exceeding those according to the preceding table.

- The block error rate (BLER) performance for USF/MCS5 to 9 not to exceed 1% at co-channel interference ratios (C/Ic) exceeding those according to the following table.

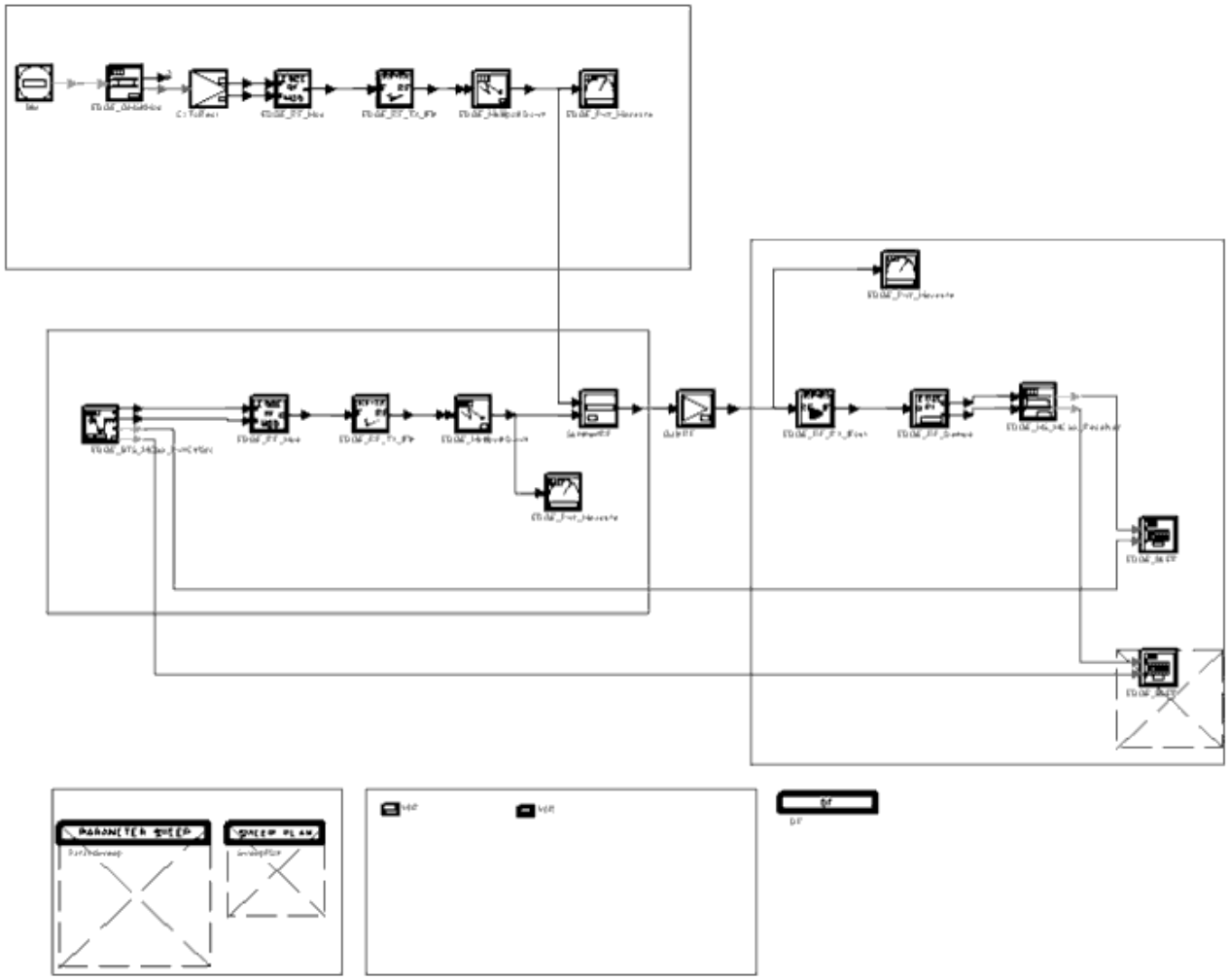
USF Co-channel Interference Ratio for 8PSK modulation

GSM 400 and GSM 900				
Type of Channel	**Propagation Conditions**			
	TUlow (no FH)	**TUhigh (no FH)**	**TUhigh (ideal FH)**	**RA (no FH)**
PDTCH MCS-5 to 9 (dB)	17	11.5	9	9

Schematic

Schematic for this design is shown in the following figure. EDGE_BTS_MCS5_PwrCtrlSrc generates the PDTCH MCS5 packages and outputs the original source data and USF as the reference for BLER calculation. The power of each time slot of the TDMA frame is controlled by this source. The branch in the upper place generates the GMSK modulated interference signal (I1). EDGE_Pwr_Measure subnetworks are used to measure power for the calibration of C/Ic. EDGE_MS_MCS5_Receiver retrieves the original source data using RSSE (reduced-state sequence estimation) and the MCS5 decode. Data and USF at the output of the receiver are then used for BLER calculation.

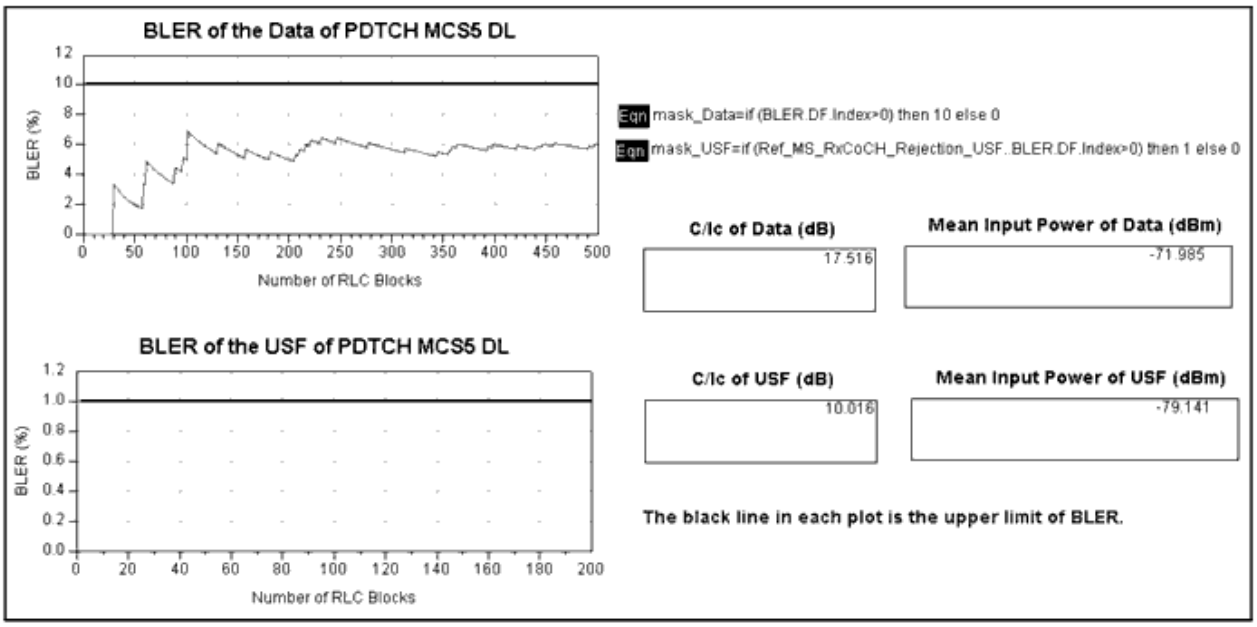
There are two EDGE_BLER subnetworks in the design for data and USF BLER.



MS_RxCoCH_Rejection Schematic

Test Results

Test results displayed in the MS_RxCoCH_Rejection.dds file are shown in the following figure. Results meet the test requirements.



MS_RxCoCH_Rejection.dds

Benchmark

PDTCH MCS5 Data

- Hardware platform: Pentium III 800 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 500 RLC blocks
- Simulation time: approximately 15 hours

PDTCH MCS5 USF

- Hardware platform: Pentium III 800 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 1000 RLC blocks
- Simulation time: approximately 29.5 hours

Adjacent Channel Rejection Measurements

MS_RxAdCH_Rejection

Features

- mobile station receiver adjacent channel selectivity measurements
- integrated RF models
- PDTCH BLER
- USF BLER
- mean power of wanted signal through a TUhigh channel
- mean power of adjacent channel interferer through a TUhigh channel

Description

This design is used to measure mobile station receiver adjacent channel sensitivity according to GSM 11.10,14.18.3 (CR: Tdoc SMG7 EDGE 031 version 4.0). MCS5 is used for this test.

Adjacent channel selectivity is a measure of the receiver's ability to receive the wanted data packets without exceeding a given degradation due to the presence of an interfering signal (I1) in the adjacent channel. The wanted signal in this test is the signal generated by the transmitted RLC data blocks.

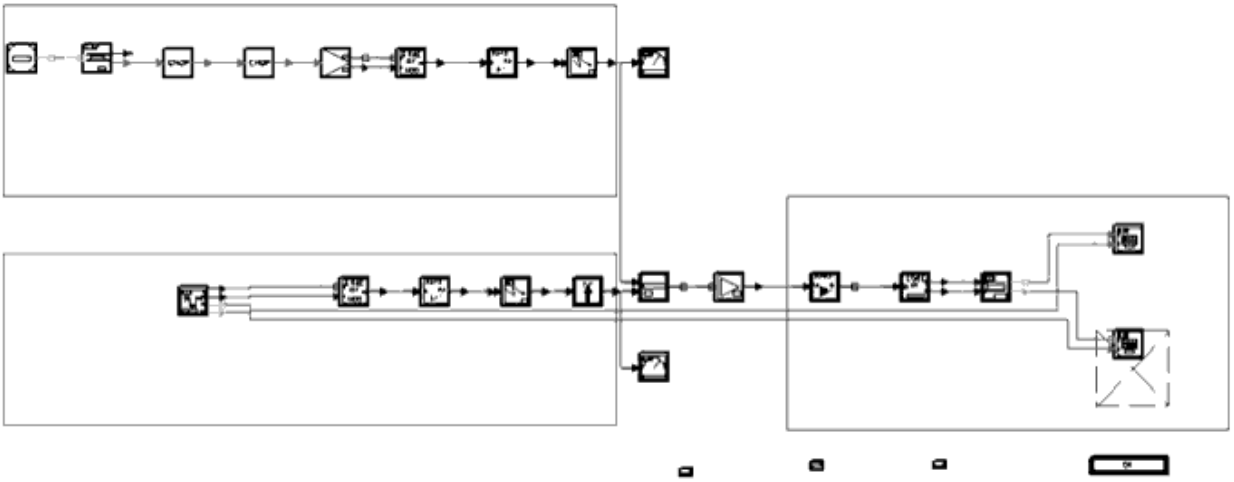
The adjacent channel can be adjacent in the RF spectrum or in time. Adjacent RF channel selectivity test is performed in this test.

- For 8PSK modulation, under adjacent channel interference at 200 kHz above and below the wanted signal frequency and at the interference ratio (C/Ia1) specified in the following table.
  - For a TUhigh faded wanted signal and a TUhigh adjacent interferer, BLER performance for PDTCH/MCS5 to 9 not to exceed 10% or 30% depending on Coding Scheme; GSM 05.05,6.2.
  - For a TUhigh faded wanted signal and a TUhigh adjacent interferer, the BLER performance for USF/MCS5 to 9 not to exceed 1%; GSM 05.05,6.2.
- For 8PSK modulation, under adjacent channel interference at 400 kHz above and below the wanted signal frequency and at the interference ratio (C/Ia2) exceeding C/Ic-50dB where C/Ic is the co-channel interference ratio
  - For a TUhigh faded wanted signal and a TUhigh adjacent interferer, the BLER performance for PDTCH/MCS5 to 9 not to exceed 10% or 30% depending on Coding Scheme; GSM 05.05,6.2.
  - For a TUhigh faded wanted signal and a TUhigh adjacent interferer, the BLER performance for USF/MCS5 to 9 not to exceed 1%; GSM 05.05,6.2.
- For a PDTCH with 8PSK modulation C/Ic is specified in the following table, for USF with 8PSK modulation C/Ic is specified in the preceding table.

8PSK Modulation Adjacent Channel Interference Ratio

GSM 400 and GSM 900					
Type of channel	**Propagation Conditions**				
	TUlow (no FH)	**TUlow (ideal FH)**	**TUhigh (no FH)**	**TUhigh (ideal FH)**	**RA (no FH)**
PDTCH/MCS-5	2.5	-2	-1	-2	1
PDTCH/MCS-6	5.5	0.5	2	1	6.5
PDTCH/MCS-7	10.5	8	10	9	†
PDTCH/MCS-8	15.5	9 † †	11 † †	10.5 † †	†
PDTCH/MCS-9	10 † †	12.5 † †	17 † †	15.5 † †	†
USF/MCS-5 to 9	-1	-8.5	-8	-9.5	-9
† Does not meet reference performance. † † Performance is specified at 30% BLER,					

Schematic

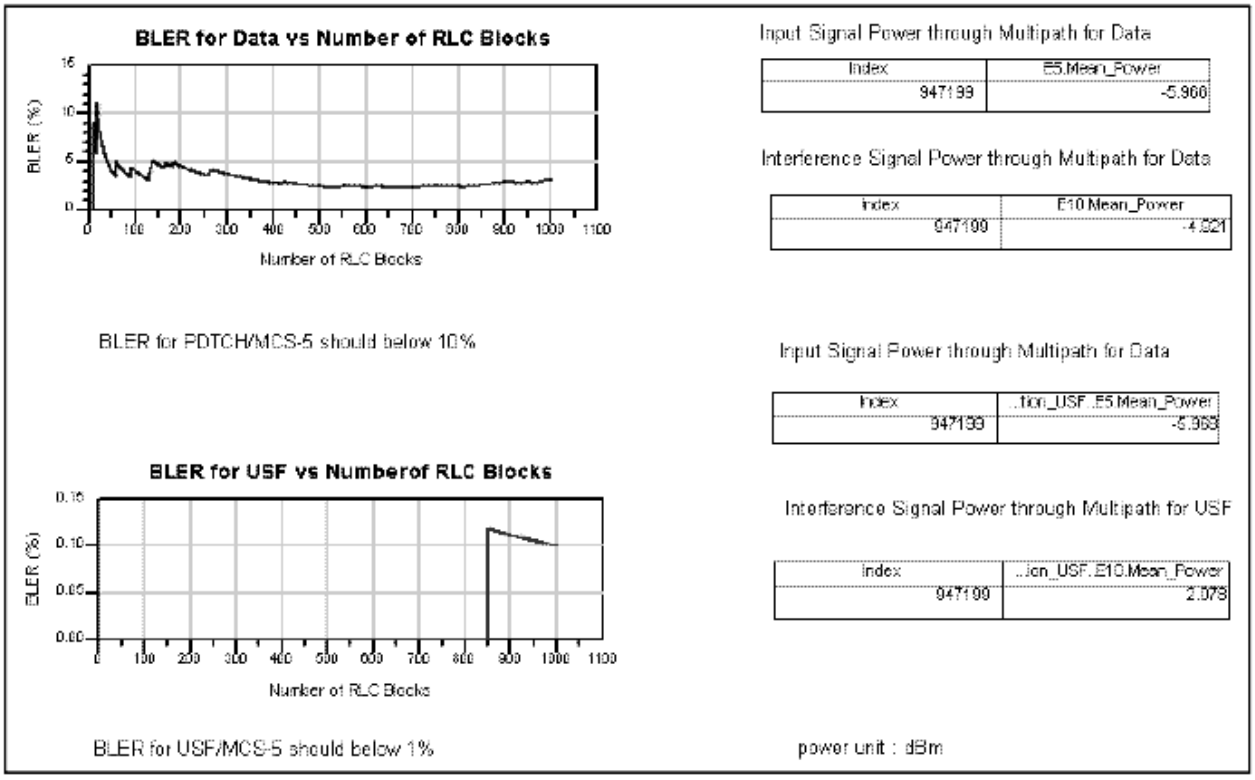


MS_RxAdCH_Rejection Schematic

Test Results

- mean power of wanted signal for PDTCH/MCS-5 through a TUhigh faded channel: −5.968 dBm
- mean power of adjacent channel interferer for PDTCH/MCS-5 through a TUhigh faded channel: −4.921 dBm
- mean power of wanted signal for USF/MCS-5 through a TUhigh faded channel: −5.968 dBm
- mean power of adjacent channel interferer for USF/MCS-5 through a TUhigh faded channel: 2.078 dBm
- BLER for PDTCH/MCS-5 (1000 RLC blocks measured): 0.3%
- BLER for USF/MCS-5 (1000 RLC blocks measured): 3.4%

The results for MCS5 displayed in the MS_RxAdCH_Rejection.dds file are shown in the following figure. Test results meet the requirements.



MS_RxAdCH_Rejection.dds

Benchmark

- Hardware platform: Pentium III 800 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Data points: 600 frames
- Simulation time:
  - approximately 13.8 hours for PDTCH/MCS-5 per 1000 RLC blocks
  - approximately 23 hours for USF/MCS-5 per 1000 RLC blocks.

Blocking Characteristics Measurements

MS_RxBlocking_Test

Features

- mobile station receiver blocking characteristics measurements
- integrated RF models
- PDTCH BLER
- USF BLER
- mean power of wanted signal at receiver input
- mean power of interferer at receiver input

Description

This design measures mobile station blocking characteristics according to GSM11.10, 14.18.5 (CR: Tdoc SMG7 EDGE 31 version 4.0). MCS9 is used for this test.

Blocking is a measure of the receiver's ability to receive a modulated wanted input signal in the presence of an unwanted input signal, on frequencies other than those of spurious responses or adjacent channels, without exceeding a given degradation. The signal in this test is the signal generated by the transmitted RLC data blocks.

Blocking characteristics of the receiver are specified separately for in-band and out-of-band performance as specified in GSM 05.05 section 5.1.

The BLER performance for PDTCH/MCS5 to 9 is not to exceed 10% or 30% depending on the coding scheme; for USF/MCS5 to 9 it is not to exceed 1% when the following signals are simultaneously input to the receiver (GSM 05.05, 6.2):

- a static 8PSK wanted signal, 4dB above the reference sensitivity level specified in the first of the following three tables for PDTCH channel and in the second table for USF.
- a continuous, static sine wave unwanted signal at a level specified in the third of the following three tables and at a frequency f which is an integer multiple of 200 kHz.

PDTCH Sensitivity Input Level for Mobile Station 8PSK Modulation

GSM 400 and GSM 900					
Type of Channel	**Propagation Conditions**				
	Static	**TUhigh (no FH)**	**TUhigh (ideal FH)**	**RA (no FH)**	**HT (no FH)**
PDTCH/MCS-5	-98 dBm	-93 dBm	-94 dBm	-93 dBm	-92 dBm
PDTCH/MCS-6	-96 dBm	-91 dBm	-91.5 dBm	-88 dBm	-89 dBm
PDTCH/MCS-7	-93 dBm	-84 dBm	-84 dBm	†	-83 dBm ††
PDTCH/MCS-8	-90.5 dBm	-83 dBm ††	-83 dBm ††	†	†
PDTCH/MCS-9	-86 dBm	-78.5 dBm ††	-78.5 dBm ††	†	†
† Cannot meet the reference performance. †† Performance is specified at 30% BLER.					

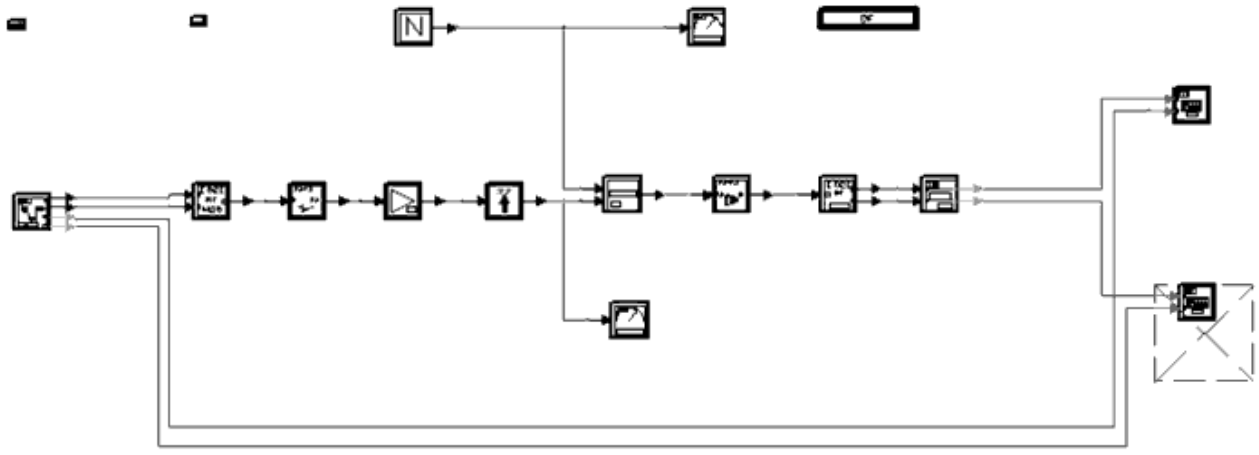
USF Sensitivity Input Level for 8PSK Modulation

GSM 400 and GSM 900					
Type of Channel	**Propagation Conditions**				
	Static	**TUhigh (no FH)**	**TUhigh (ideal FH)**	**RA (no FH)**	**HT (no FH)**
USF/MCS-5 to 9	-102 dBm	-97.5 dBm	-99 dBm	-100 dBm	-99 dBm

Level of Unwanted Signals

Frequency	**GSM900**	
	Small MS	**Other MS**
	Level in dBµVemf( )	
FR +/- 600 kHz to FR +/- 800 kHz	70	75
FR +/- 800 kHz to FR +/- 1,6 MHz	70	80
FR +/- 1,6 MHz to FR +/- 3 MHz	80	90
915 MHz to FR - 3 MHz	90	90
FR + 3 MHz to 980 MHz	90	90
835 MHz to <915 MHz	113	113
>980 MHz to 1000 MHz	113	113
100 kHz to <835 MHz	90	90
>1000 MHz to 12,750 MHz	90	90

Schematic

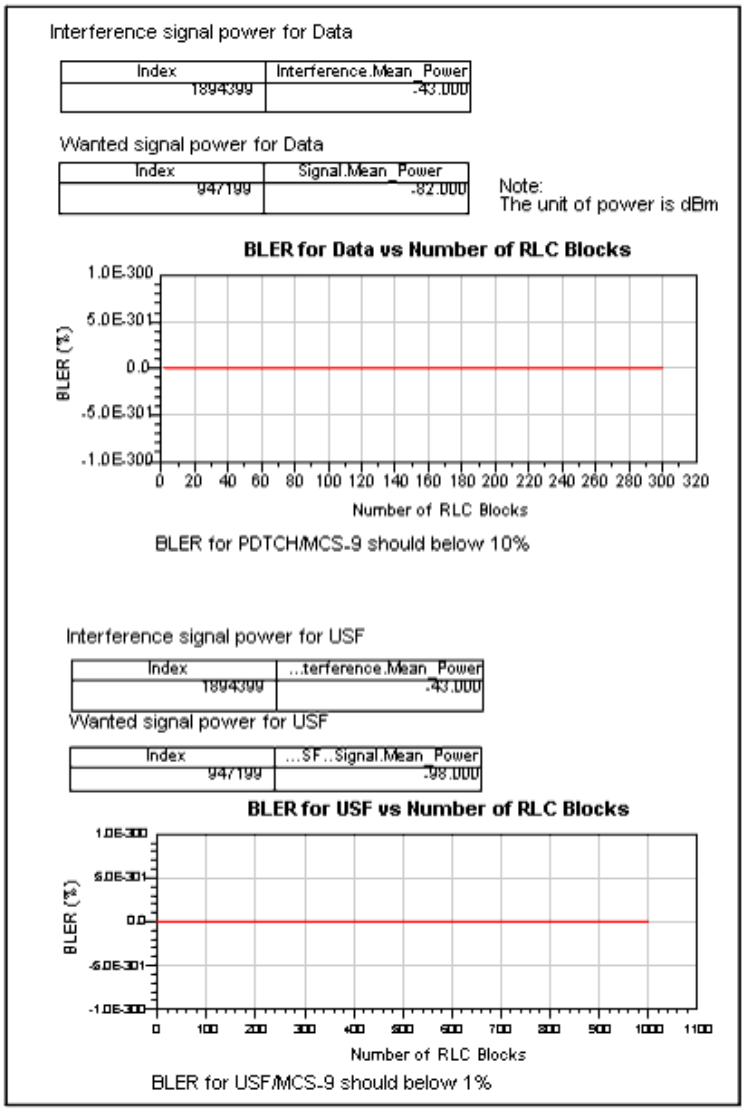


MS_RxBlocking_Test Schematic

Test Results

- mean power of wanted signal for PDTCH/MCS-9: −82.000 dBm
- mean power of interferer PDTCH/MCS-9: −43.000 dBm
- mean power of wanted signal for USF/MCS-9: −98.000 dBm
- mean power of interferer USF/MCS-9: −43.000 dBm
- BLER for PDTCH/MCS-9 (300 RLC blocks measured): 0.0%
- BLER for USF/MCS-9 (1000 RLC blocks measured): 0.0%

The test results for MCS9 displayed in the MS_RxBlocking_Test.dds file are shown in the following figure. The results meet the requirements.



MS_RxBlocking_Test.dds

Benchmark

- Hardware platform: Pentium II 450 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Data points: 1000 RLC Blocks
- Simulation time:
  - approximately 6 hours for PDTCH/MCS-9 per 300 RLC blocks
  - approximately 17 hours for USF/MCS-9 per 1000 RLC blocks

EDGE Mobile Station Transmitter Design Examples

Introduction

The MS_TX_wrk workspace provides design examples of mobile station transmitter measurements including 8PSK frequency error and modulation accuracy, EGPRS transmitter output power, and output RF spectrum in EGPRS configuration. Measurements are based on GSM 11.10 section 13.17 and corresponding EDGE *Change Request* documents.

Design examples include:

- 8PSK frequency error and modulation accuracy: MS_TxEVM_2pin and MS_TxFreqErr.
- EGPRS transmitter output power: MS_TxOutputPwr and MS_TxPwr_vs_Time.
- Output RF spectrum in EGPRS configuration: MS_TxORFS_Step1 and MS_TxORFS_Step2.

Designs in this workspace consist of:

- User equipment signal source in baseband
  EDGE_ActiveIdleSrc provides framed and modulated baseband signal for EDGE. EDGE_RandomSrc provides continuous, random and modulated baseband signal for EDGE
- Transmission modulation and up-converter
  Data from the baseband signal source for EDGE is up-converted to a 71 MHz RF signal with EDGE_RF_Mod, then modulated into an 890 MHz RF signal with EDGE_RF_TX_IFin.

8PSK Modulation Accuracy for 2-pin EVM

EDGE_MS_TX_wrk Design Name

- MS_TxEVM_2pin

Features

- 2-pin EVM model
- RMS, peak, and 95th percentile EVM measurements
- 8PSK modulation with pulse shaping filter and continuous $\frac{3}{8}\pi$ symbol phase rotation
- adjustable sample rate
- integrated RF section
- Circuit envelope co-simulation for RF transmitter
- EDGE measurement filter (raised-cosine-windowed-raised-cosine filter)

Description

This design illustrates mobile station 8PSK modulation accuracy by measuring the EVM. The 2-pin EVM model is used that requires ideal transmitted signals as reference input. Frequency error, origin offset suppression, as well as evaluations of modulation accuracy, are measured in MS_TxFreqErr.

Measurements in this design are based on GSM 11.10 section 13.17.1 and the corresponding *Change Request* .

Test requirements are:

- RMS EVM not to exceed 9.0%
- (averaged) value of peak EVM not to exceed 30%
- 95th percentile value not to exceed 15%

For the EVM measurement, the transmitted signal is modeled by

$$Y(t) = C1\{R(t) + D(t) + C0\}Wt$$

where

R(t) is defined to be an ideal transmitter signal (reference signal)

D(t) is the residual complex error on signal R(t)

C0 is a constant origin offset representing carrier feed-through

C1 is a complex constant representing the arbitrary phase and output power of the transmitter

W = $e^{\alpha + j2\pi f}$ accounts for a frequency offset of 2πf radians per second phase rotation and an amplitude change of α nepers per second

The symbol timing phase of Y(t) is aligned with R(t).

The transmitted signal Y(t) is compensated in amplitude, frequency and phase by multiplying with the factor:

W-t/C1

Values for W and C1 are determined using an iterative process. W(α,f), C1 and C0 are chosen to minimize the RMS value of EVM.

After compensation, Y(t) is passed through the specified measurement filter (GSM 05.05, 4.6.2) to produce the signal

Z(k) = S(k) + E(k) + C0

where

S(k) is the ideal transmitter signal observed through the measurement filter

k = floor (t/T_s), where T_s =1/270.833kHz corresponding to the symbol times

The error vector is defined to be

E(k) = Z(k) - C0 -S(k)

It is measured and calculated for each instant k over the useful part of the burst excluding tail bits. The RMS vector error is defined as:

$$\text{RMS EVM} = \sqrt{\sum_{k \in K} |E(k)|^2 / \sum_{k \in K} |S(k)|^2}$$

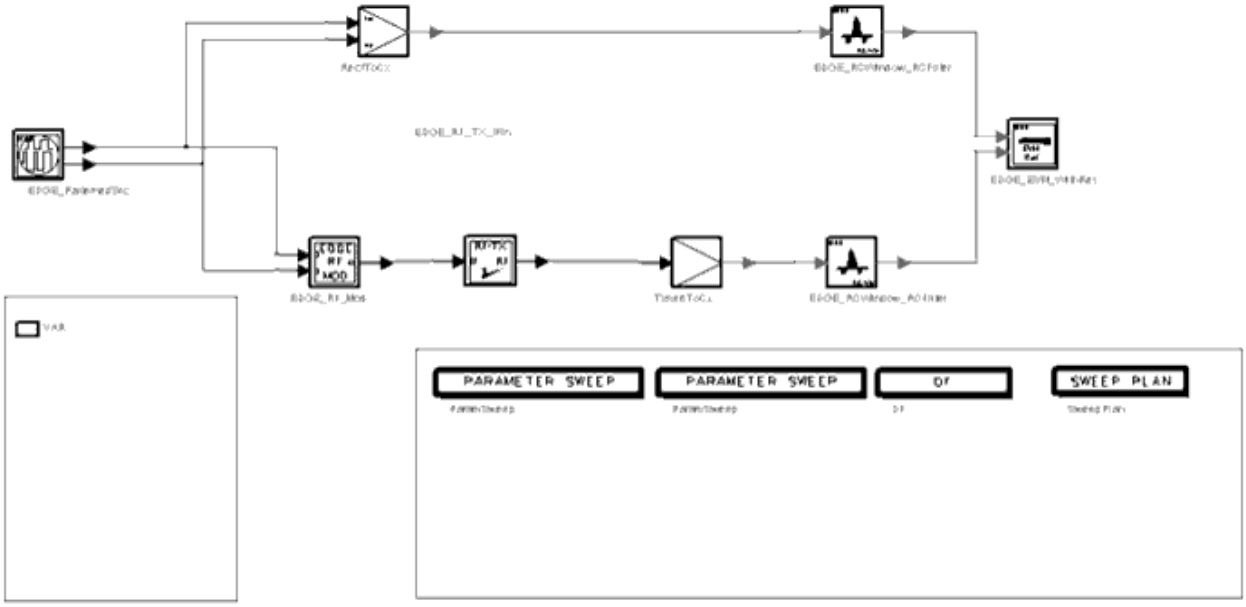
The peak EVM is the peak error deviation within a burst, measured at each symbol interval, averaged over at least 200 bursts.

The 95th percentile EVM is the point where 95% of the individual EVM, measured at each symbol interval, is below that point. That is, only 5% of the symbols are allowed to have an EVM exceeding the 95th percentile point. EVM values are obtained during the useful part of the burst (excluding tail bits) over 200 bursts.

Schematic

The schematic for this design is shown in the following figure. EDGE_RandomSrc is a continuous random source generating 8PSK modulated signals. The upper path is for the reference signal. The raised-cosine-windowed raised cosine filters used before EDGE_FrequencyErr are the EDGE measurement filters. In EDGE_EVM_WithRef NumBursts is set to 200 to get the averaged results over 200 bursts; SymBurstLen is set to 142, which is derived from the following equation:

142 (length of useful part) = 156 (length of whole burst) -8 (guard symbols) -6 (tail symbols)



MS_TxEVM_2pin Schematic

Test Results

EVM Results for MS Transmitter

	ARFCN 1 (%)	ARFCN 63 (%)	ARFCN 124 (%)
RMS EVM	5.945	6.020	5.800
Peak EVM	11.676	11.621	11.256
95:th percentile EVM	9.723	9.788	9.401

Upper limit of the test requirement for RMS EVM is 9.0%.

Upper limit of the test requirement for peak EVM is 30.0%.

Upper limit of the test requirement for 95:th percentile EVM is 15.0%.

Benchmark

- Hardware platform: Pentium II 400 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 9 × 200 bursts (9 × 142 × 200 = 255600 symbols)

- Simulation time: approximately 100 minutes

8PSK Frequency Error and Modulation Accuracy

EDGE_MS_TX_wrk Design Name

- MS_TxFreqErr

Features

- Frequency error and origin offset suppression of 8PSK modulation measured
- 8PSK modulation with pulse shaping filter and continuous $\frac{3}{8}\pi$ symbol phase rotation
- Sample rate adjustable
- RF section integrated
- Circuit envelope co-simulation for RF transmitter
- EDGE measurement filter (raised-cosine-windowed-raised-cosine filter)

Description

This design shows the evaluation of the mobile station 8PSK modulation accuracy by measuring the frequency error and OOS (origin offset suppression). The 2-pin EDGE_FrequencyErr model is used, which needs ideal transmitted signals as reference input. Frequency error and origin offset suppression, as the EVM is, are evaluations of modulation accuracy.

Tests in this design are implemented according to the methods and requirements described in 13.17.1 of GSM 11.10 and the corresponding *Change Request* .

Test requirements are:

- frequency error < 0.1 ppm
  (for GSM 900: < $900 \times 10^{6} \times 0.1 \times 10^{-7}$ = 90 Hz)
- OOS > 30 dB.

Frequency Error and OOS Calculation

The transmitted signal is modeled by:

Y(t) = C1{R(t) + D(t) + C0}Wt

R(t) is defined to be an ideal transmitter signal (reference signal)

D(t) is the residual complex error on signal R(t)

C0 is a constant origin offset representing carrier feed-through

C1 is a complex constant representing the arbitrary phase and output power of the transmitter

W = $e^{\alpha + j2\pi f}$ accounts for both a frequency offset of "2πf" radians per second phase rotation and an amplitude change of "α" nepers per second

Symbol timing phase of Y(t) is aligned with R(t).

The transmitted signal Y(t) is compensated in amplitude, frequency and phase by multiplying with the factor:

W-t/C1

Values for W and C1 are determined using an iterative procedure. W(α,f), C1 and C0 are chosen to minimize the RMS value of EVM.

After compensation, Y(t) is passed through the specified measurement filter (GSM 05.05, 4.6.2) to produce the signal

Z(k) = S(k) + E(k) + C0

where

S(k) is the ideal transmitter signal observed through the measurement filter

k = floor (t/Ts), where Ts =1/270.833 kHz corresponding to the symbol times

The frequency error is defined as the f of W = $e^{\alpha + j2\pi f}$.
OOS is defined as

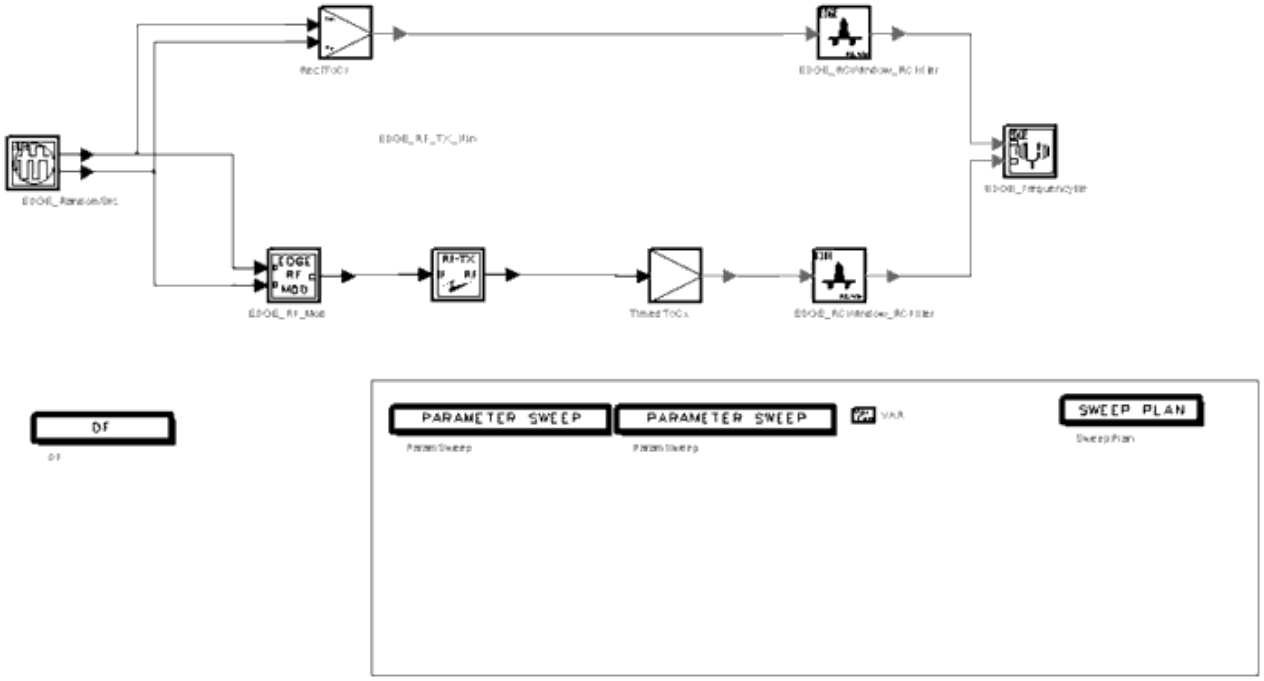
$$OOS(dB) = -10\log_{10}\left(\frac{|C_0|^2}{\frac{1}{N}\sum_{k \in K}|S(k)|^2}\right)$$

Schematic

The schematic for this design is shown in the following figure. EDGE_RandomSrc is a continuous random source generating 8PSK modulated signals. The upper path is for the reference signal. The raised-cosine-windowed raised cosine filters used before the EDGE_FrequencyErr are the EDGE measurement filter. NumBursts is set to 200 to obtain the averaged results over 200 bursts. SymBurstLen is set to 142, which is derived from the equation

142 (length of useful part) = 156 (length of whole burst)

−8 (guard symbols) −6 (tail symbols)



MS_TxFreqErr Schematic

Test Results

All results meet the test requirements.

- Frequency error (Hz): -0.422 (at ARFCN 1); -0.779 (at ARFCN 63); 0.121 (at ARFCN 124).
- Origin offset suppression (dB): 68.907 (at ARFCN 1); 68.809 (at ARFCN 63); 67.987 (at ARFCN 124).

Benchmark

- Hardware platform: Pentium II 450 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, Advanced Design System 1.3
- Data points: 6 × 200 bursts (6 × 142 × 200 = 85200 symbols)
- Simulation time: one hour

EGPRS Transmitter Mean Output Power

EDGE_MS_TX_wrk Design Name

- MS_TxOutputPwr

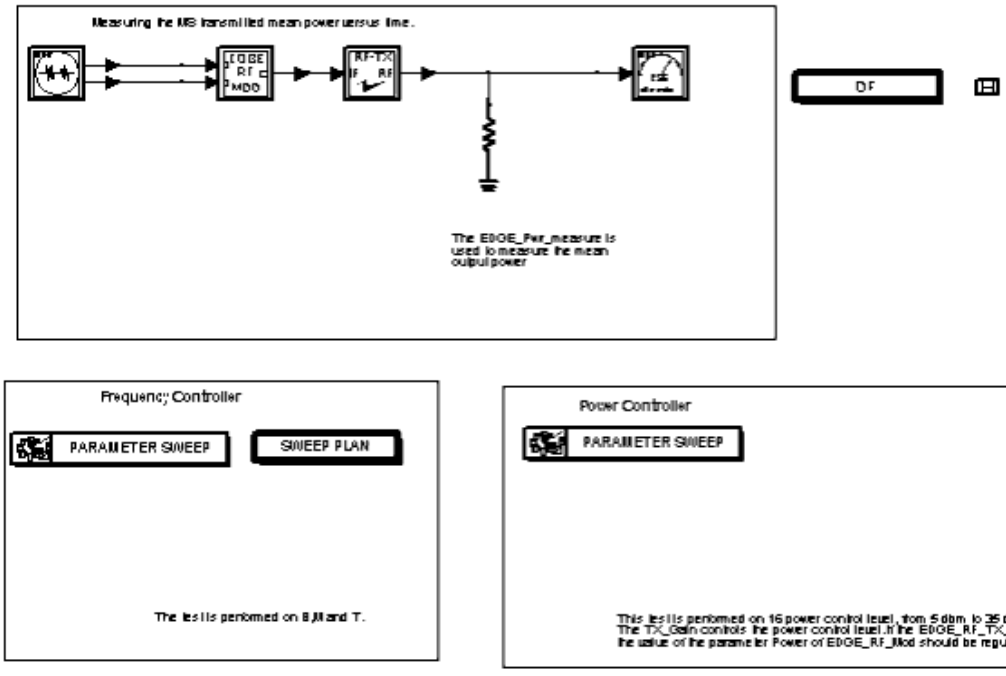
Features

- 8PSK modulation
- normal burst
- 15 power control levels from 5 dBm to 33 dBm
- adjustable sample rate
- integrated RF section

Design Description

MS_TxOutputPwr measures the mobile station mean transmitter output power to verify that all power control levels have the required output power. The schematic is shown in the following three figures.

The upper and lower masks of various control levels are calculated according to tolerances listed in the following table while the mean output power is measured. Power control levels for 8PSK (GSM400 and GSM800) must have nominal output power levels as defined in the following table, from the lowest control level to the maximum output power.



Ms_TxOutputPwr Schematic

Ms_TxOutputPwr Schematic

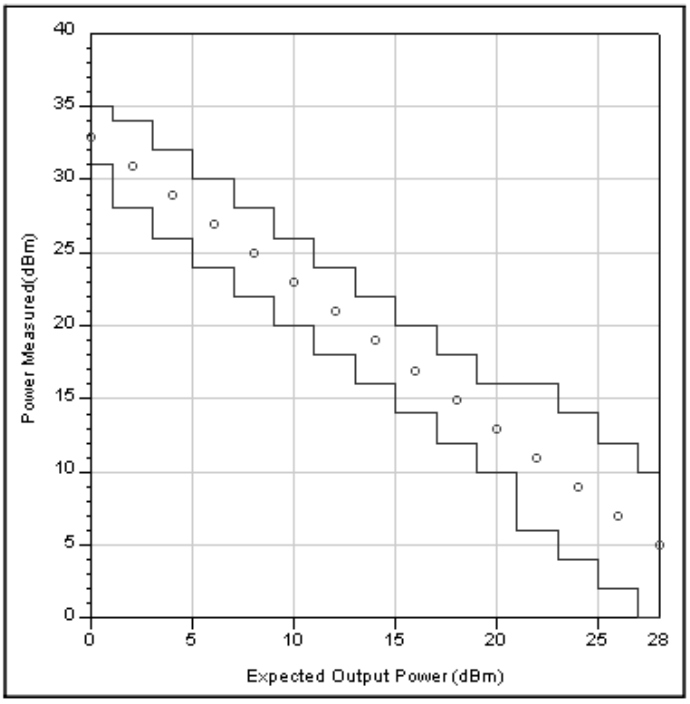
GSM400 and GSM 800 Transmitter Output Power (8PSK)

Power Control Level	Transmitter Output Power (dBm)	Normal Tolerances
5	33	+/-2dB
6	31	+/-3dB
7	29	+/-3dB
8	27	+/-3dB
9	25	+/-3dB
10	23	+/-3dB
11	21	+/-3dB
12	19	+/-3dB
13	17	+/-3dB
14	15	+/-3dB
15	13	+/-3dB
16	11	+/-5dB
17	9	+/-5dB
18	7	+/-5dB
19	5	+/-5dB

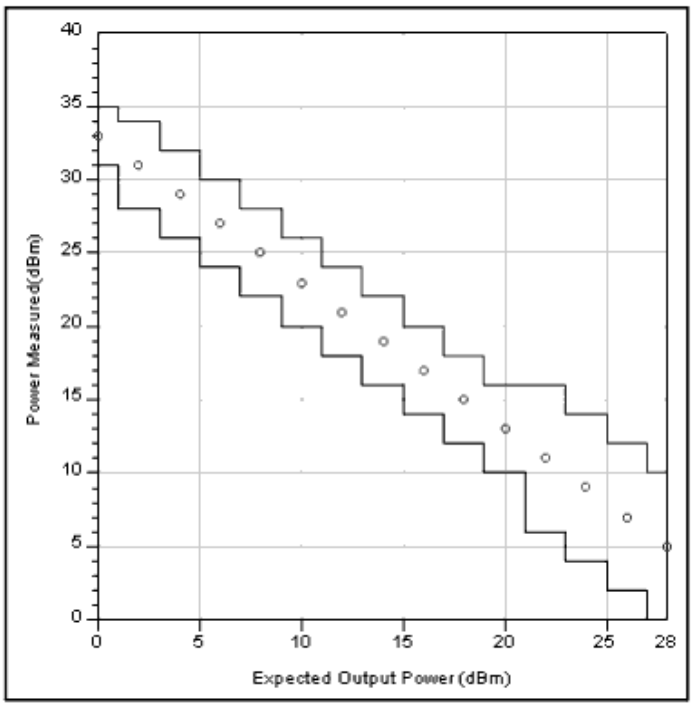
Test Results

Test results are shown in the following three figures for the lowest (890.2 MHz), middle (902.6 MHz), and highest (914.8 MHz) frequencies for which the test is performed. These figures are displayed in the MS_TxOutputPwr.dds file in a data display window; blue lines represent the upper masks while black lines represent the lower masks; circular symbols represent the output mean power.

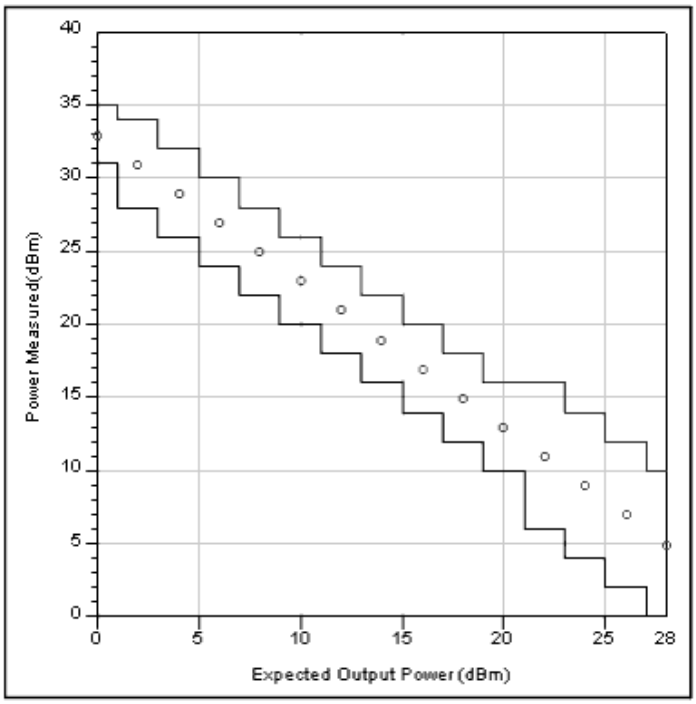
Transmitter output mean power of this design is within range of the requirements.



Mean Power for 890.2 MHz Frequency



Mean Power for 902.6 MHz Frequency



Mean Power for 914.8 MHz Frequency

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, ADS 1.3
- Time slots to be averaged: 200 time slots
- Simulation Time: approximately 18 hours

EGPRS Transmitter Output Power Versus Time

EDGE_MS_TX_wrk Design Name

- MS_TxPwr_vs_Time

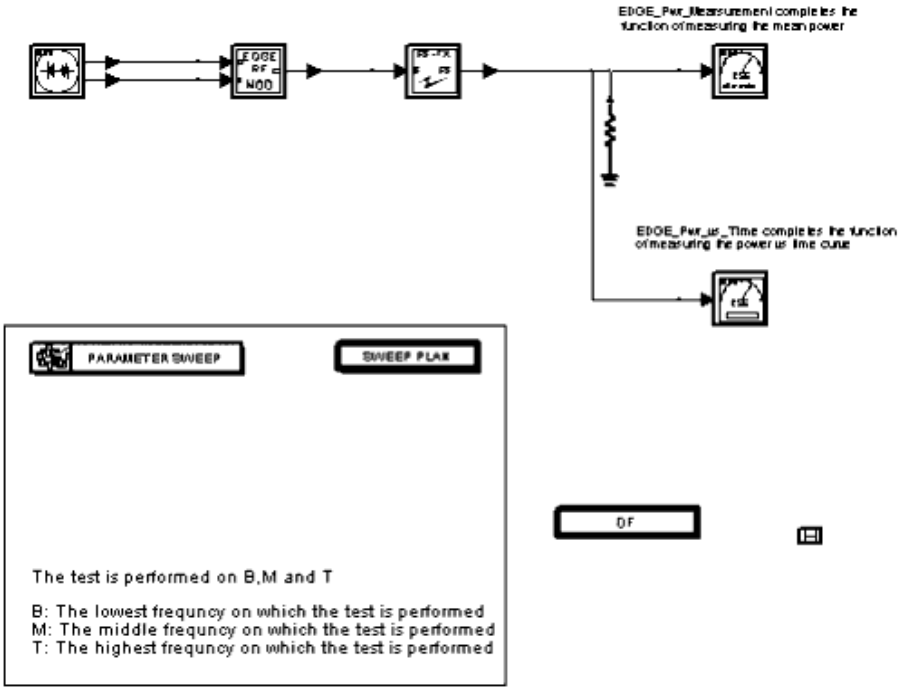
Features

- 8PSK modulation
- Normal burst
- Sample rate adjustable
- RF section integrated

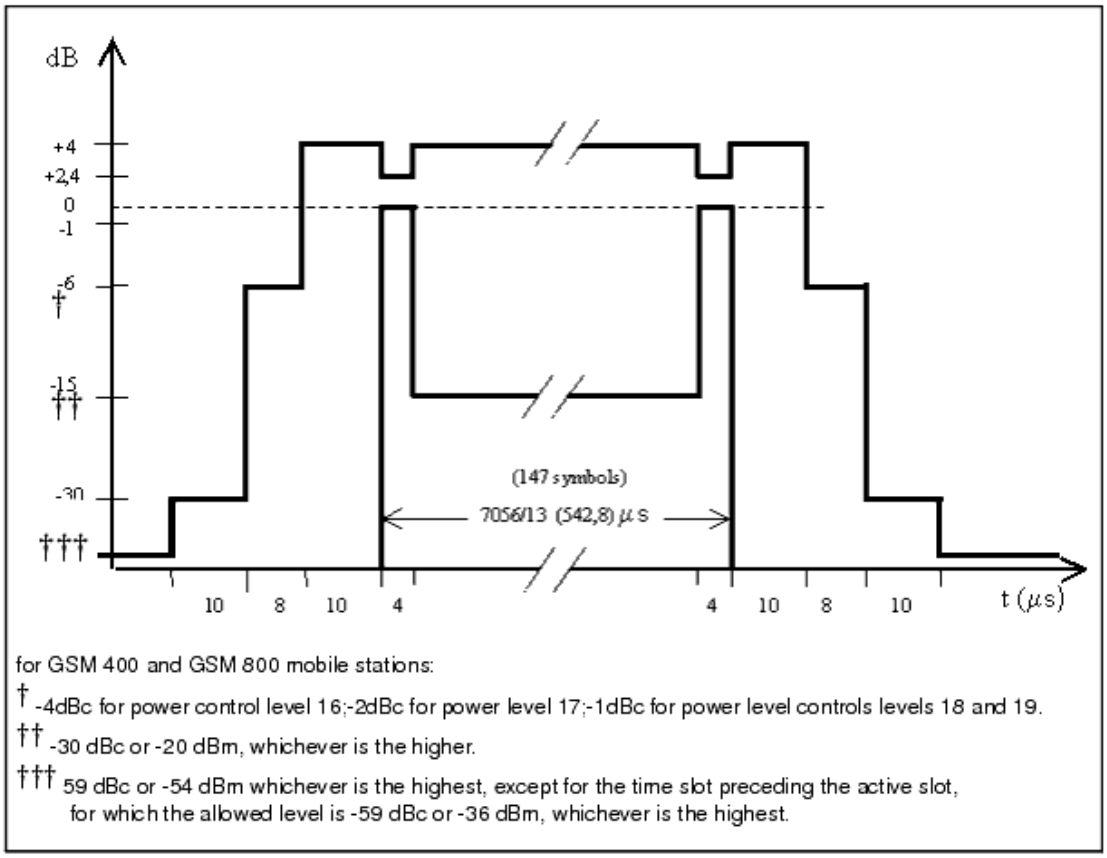
Design Description

This example measures mobile station output power versus time. This test is to verify that the output power relative to time is within the requirements for sending a normal burst of 8PSK modulated signals. The schematic for this design is shown in the first of the following two figures.

The transmitter power level relative to time for a normal burst must be within the power/time template illustrated in the second of the following two figures. In this test, the power control level is set to be 16.



Ms_TxPwr_vs_Time Schematic

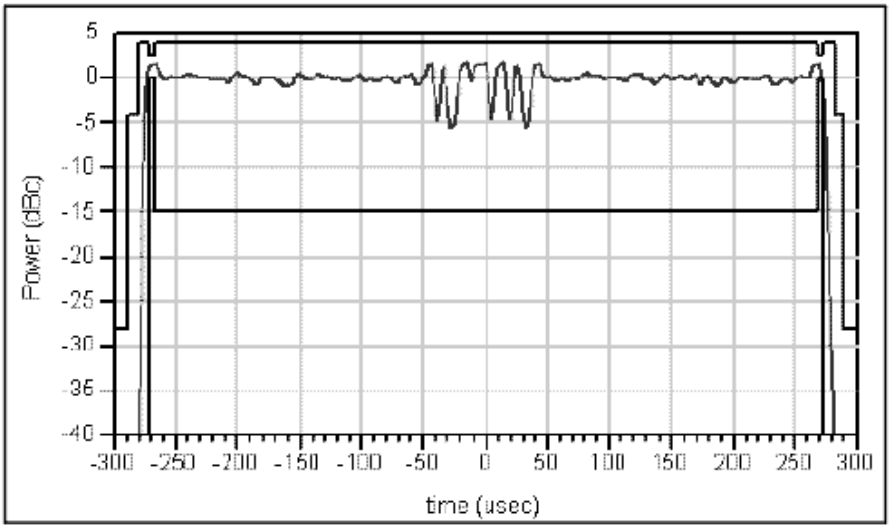


Time Mask for Normal Duration Bursts at 8PSK Modulation

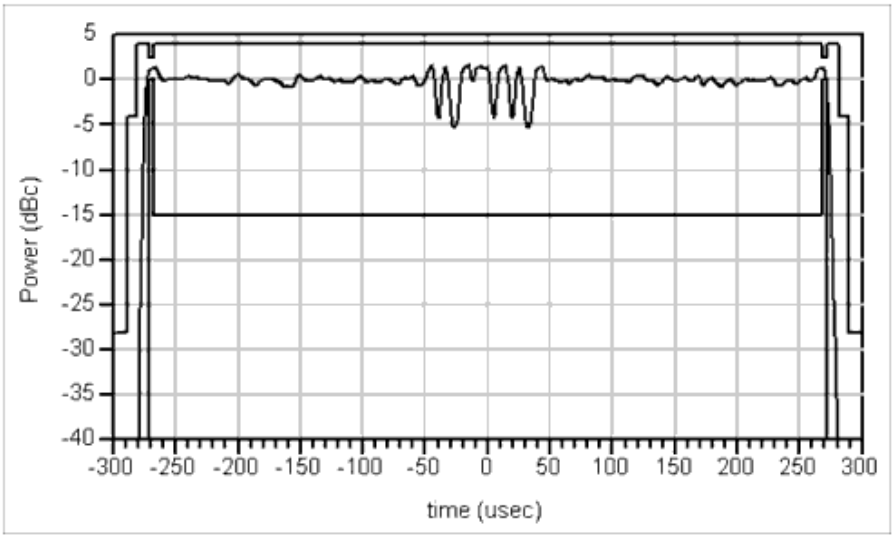
Test Results

Test results are shown in the following three figures for the lowest (890.2 MHz), middle (902.6 MHz), and highest (914.8 MHz) frequencies for which the test is performed.

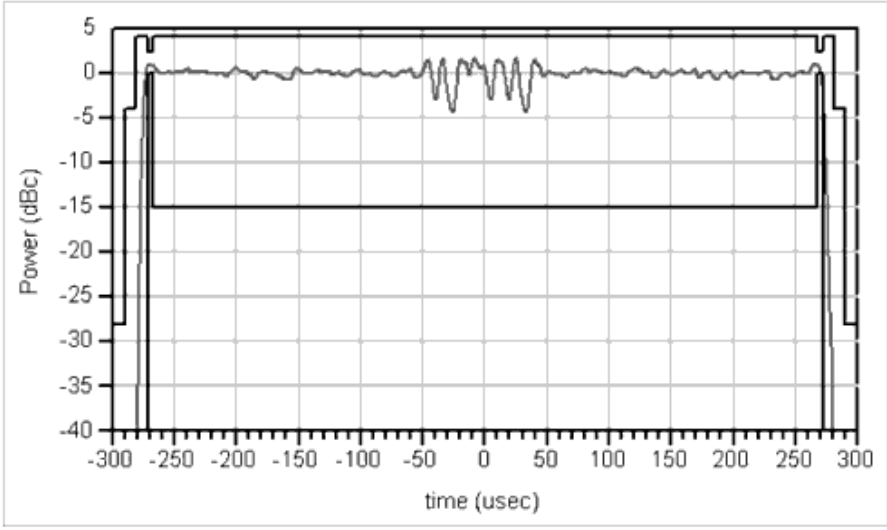
The transmitter output power versus time is within the requirements.



Power Versus Time at 890.2 MHz



Power Versus Time at 902.6 MHz



Power Versus Time at 914.8MHz

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, ADS 1.3
- Time Slots to be averaged: 200 time slots
- Simulation Time: approximately 1 hour

Output RF Spectrum in EGPRS with Modulation and Wideband Noise

EDGE_MS_TX_wrk Design Name

- MS_TxORFS_Step1
- MS_TxORFS_Step2

Features

- 8PSK modulation with pulse shaping filter and continuous $\frac{3}{8}\pi$ symbol phase rotation
- adjustable sample rate
- spectrum analysis and constellation display
- integrated RF section

Description

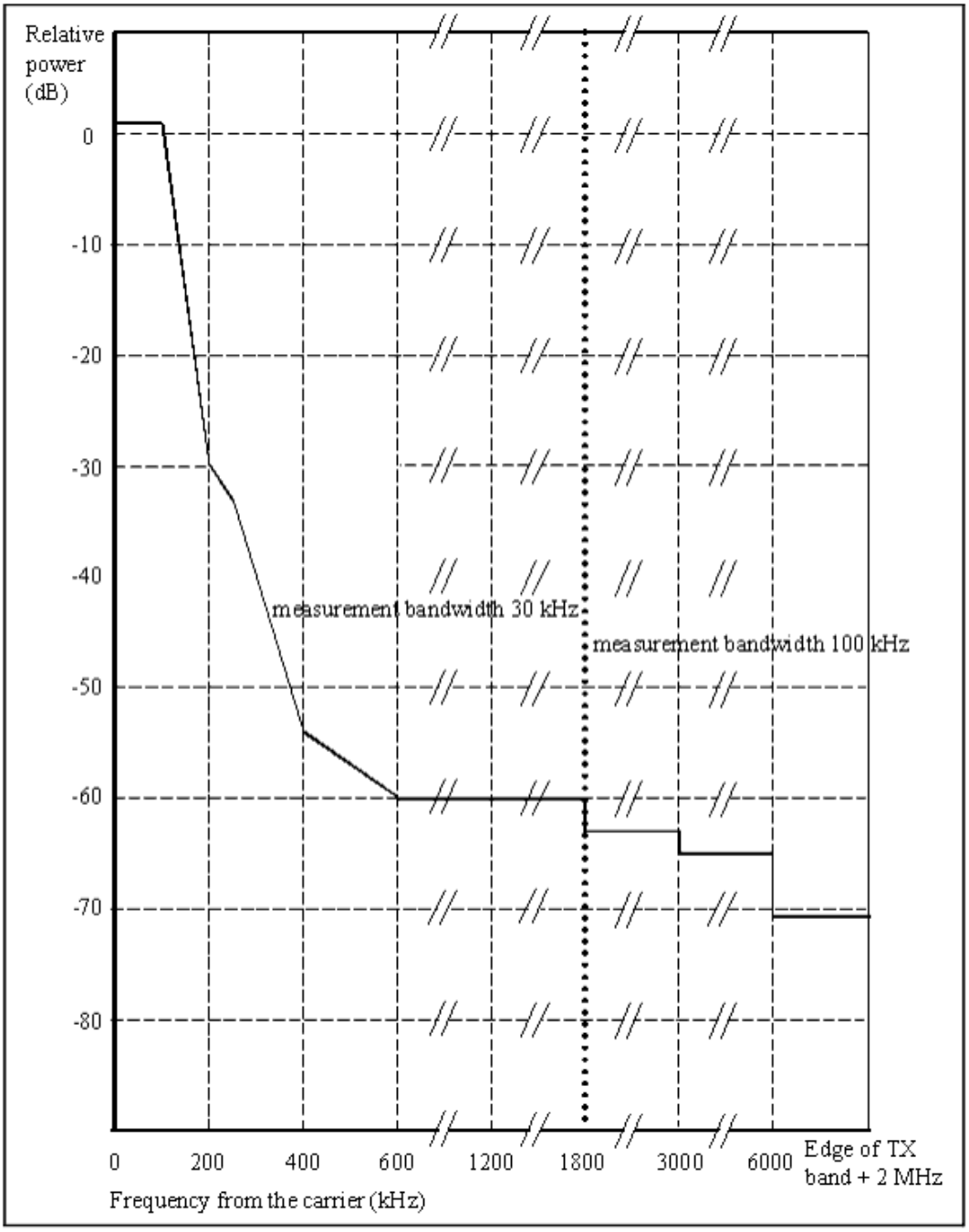
This example demonstrates the mobile station signal spectrum due to the modulation and wideband noise. The output RF modulation spectrum specifications are listed in the following table; a mask representation of these specifications is shown in the following figure.

The specification shall be met under the following measurement conditions:

> Zero frequency scan, bandwidth filter and video bandwidth of 30 to 1800 kHz, with averaging done over 50 to 90 percent of the useful part of the transmitted bursts (excluding the midamble) then averaged over at least 200 such burst measurements. Above 1800 kHz from the carrier, only measurements centered on multiples of 200 kHz are taken with averaging over 50 bursts.

GSM 400, 850, and 900 Mobile Station Specifications

Power Level	100	200	250	400	>= 600 <1800	>= 1800 <3000	>= 3000 <6000	>= 6000
≥ 39	+0.5	-30	-33	-60	-66	-69	-71	-77
37	+0.5	-30	-33	-60	-64	-67	-69	-75
35	+0.5	-30	-33	-60	-62	-65	-67	-73
≤ 33	+0.5	-30	-33	-60 †	-60	-63	-65	-71
† For equipment supporting 8PSK, the requirement for 8PSK modulation is -54 dB								

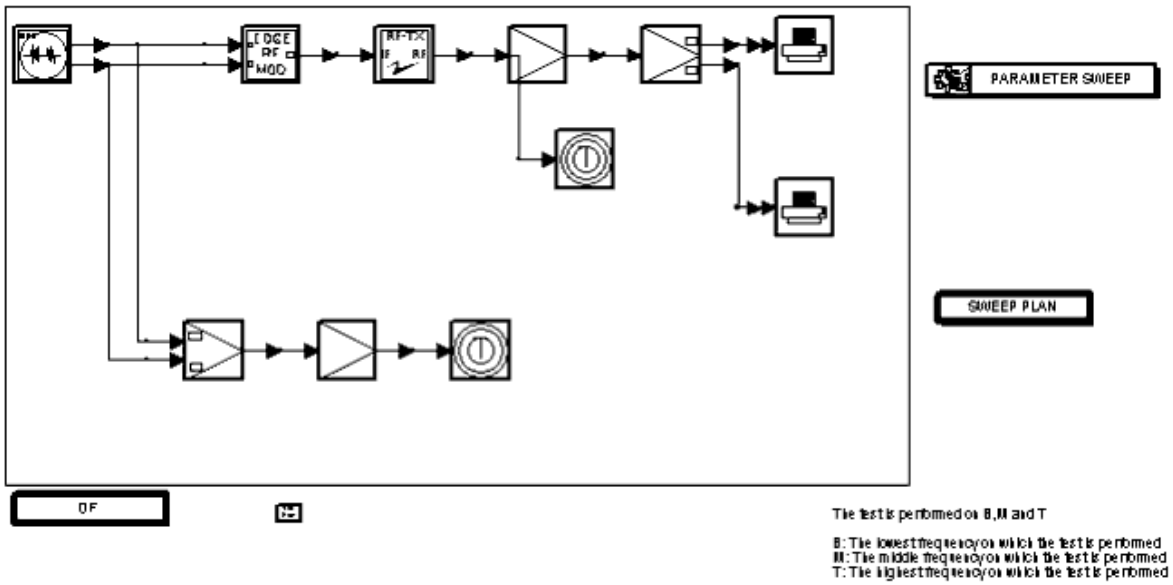


GSM 400 and GSM 900 and MXM 850

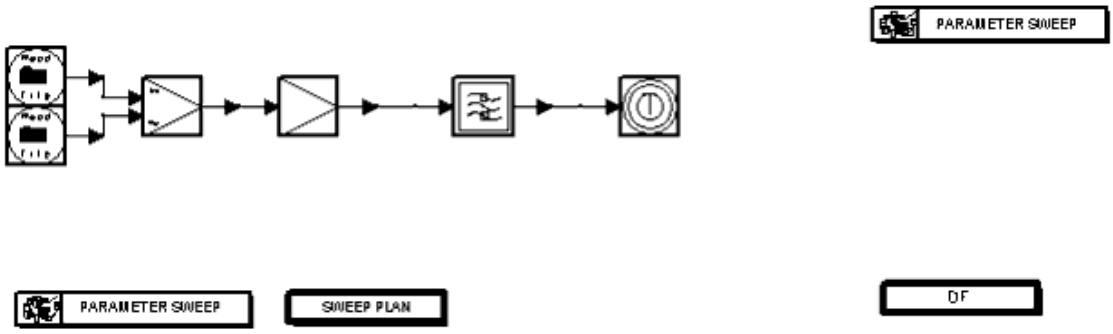
Mobile Station Spectrum at 8PSK modulation

Schematic

Design MS_TxORFS_Step1 and MS_TxORFS_Step2 are used for tests of spectrum due to modulation and switching transients.



MS_TxORFS_Step1 Schematic

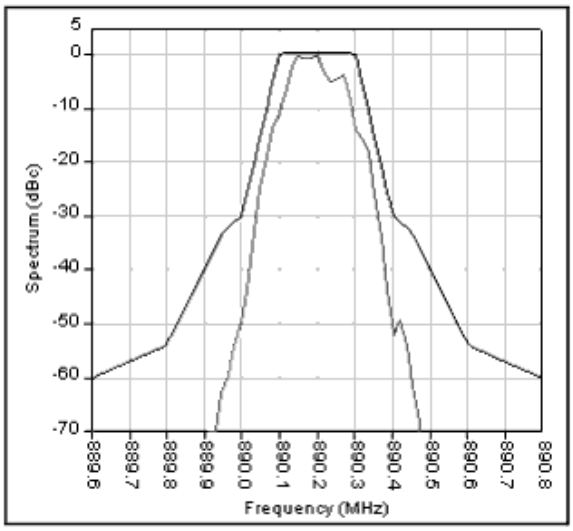


MS_TxORFS_Step2 Schematic

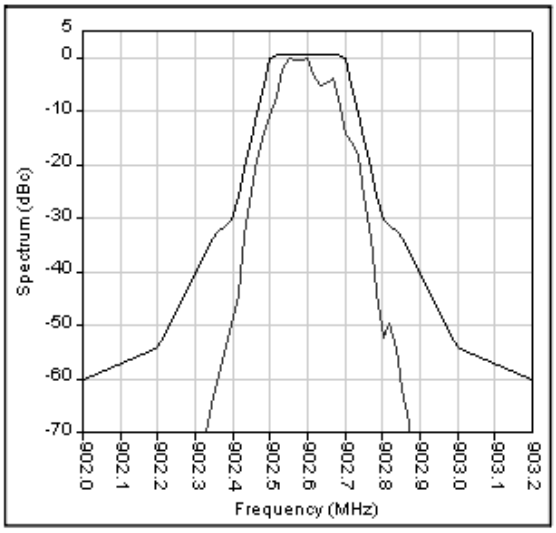
Test Results

Only the data display template is provided in this workspace, but not the simulation results because the dataset (MS_TxORFS_Step2.ds) is too large to be included in the package. To get the MS_TxORFS_Step2.ds and see the result curves, just run the designs MS_TxORFS_Step1 and then MS_TxORFS_Step2.

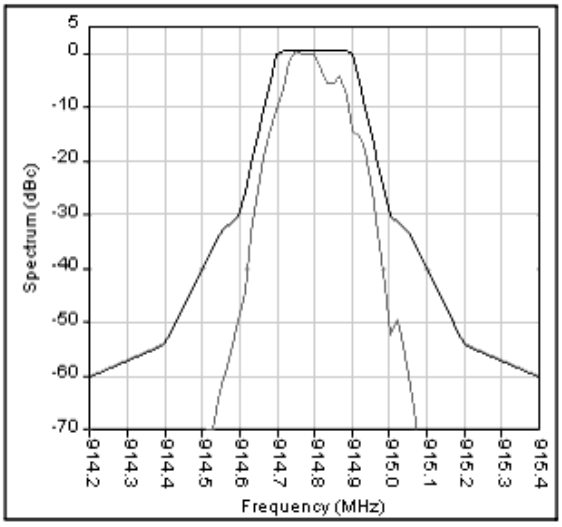
Test results shown in the following three figures are provided for reference, which are for the lowest (890.2 MHz), middle (902.6 MHz), and highest (914.8 MHz) frequencies respectively. The mask corresponds to power level 33 in the preceding table.



Output RF Spectrum, 890.2 MHz Modulation



Output RF Spectrum, 902.6 MHz Modulation



Output RF Spectrum, 914.8 MHz Modulation

Benchmark

- Hardware platform: Pentium II 400 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Data points: 1 time slot
- Simulation time: 25 seconds

Output RF Spectrum in EGPRS with Switching Transients

EDGE_MS_TX_wrk Design Name

- MS_TxORFS_Step1
- MS_TxORFS_Step2

Features

- 8PSK modulation with pulse-shaping filter and continuous $\frac{3}{8}\pi$ symbol phase rotation
- adjustable sample rate
- spectrum analysis
- integrated RF section

Description

This example shows the spectrum of the signal from the mobile station due to the switching transients (power ramping up and down). The output RF modulation spectrum is given in the following table.

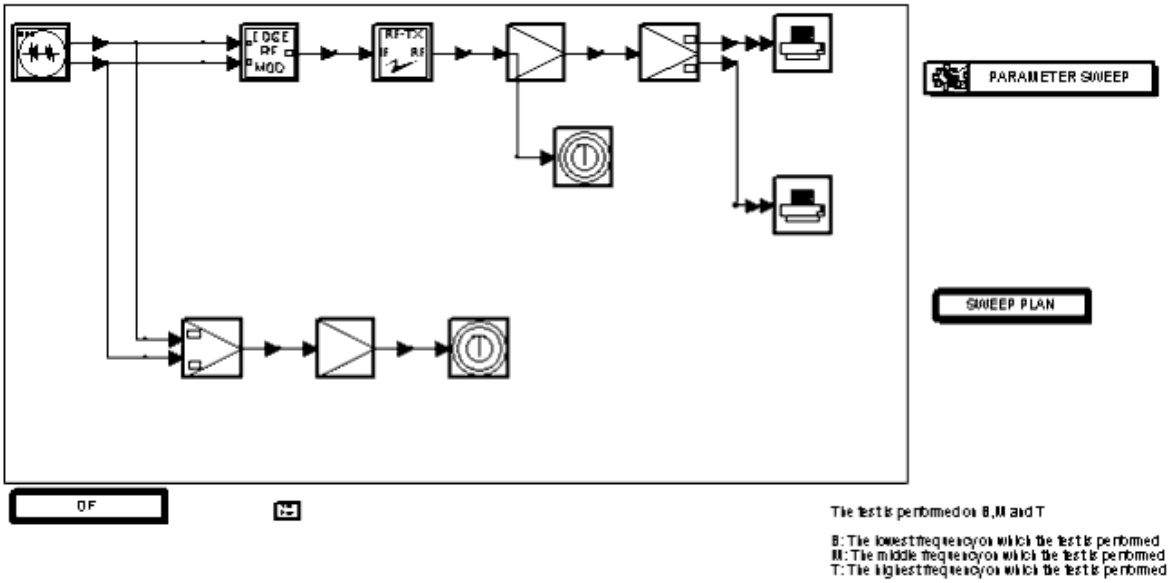
Test requirements are: zero frequency scan, 30 kHz filter bandwidth, peak hold, and 100 kHz video bandwidth.

GSM 400 and GSM 900 and GSM 850 MS

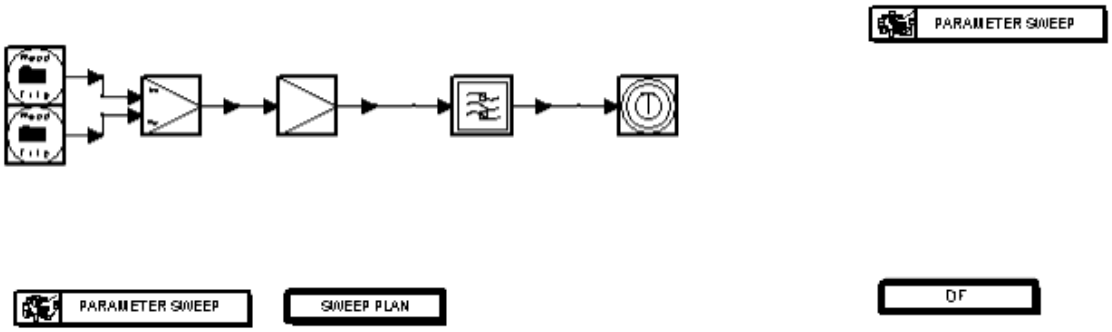
Power level	Maximum Level for Carrier Frequency Offsets			
	400 kHz	600 kHz	1200 kHz	1800 kHz
39 dBm	-13 dBm	-21 dBm	-21 dBm	-24 dBm
37 dBm	-15 dBm	-21 dBm	-21 dBm	-24 dBm
35 dBm	-17 dBm	-21 dBm	-21 dBm	-24 dBm
33 dBm	-19 dBm	-21 dBm	-21 dBm	-24 dBm
31 dBm	-21 dBm	-23 dBm	-23 dBm	-26 dBm
29 dBm	-23 dBm	-25 dBm	-25 dBm	-28 dBm
27 dBm	-23 dBm	-26 dBm	-27 dBm	-30 dBm
25 dBm	-23 dBm	-26 dBm	-29 dBm	-32 dBm
23 dBm	-23 dBm	-26 dBm	-31 dBm	-34 dBm
≤ +21 dBm	-23 dBm	-26 dBm	-32 dBm	-36 dBm

Schematics

Design MS_TxORFS_Step1 and MS_TxORFS_Step2 are used for tests of spectrum due to modulation and switching transients.



MS_TxORFS_Step1 Schematic

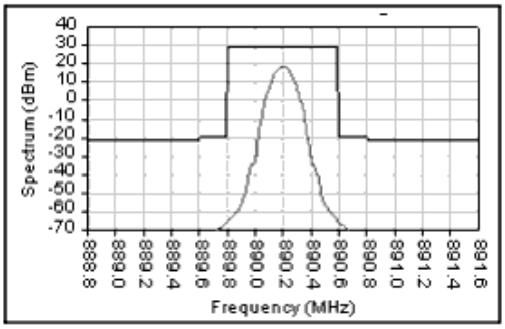


MS_TxORFS_Step2 Schematic

Test Results

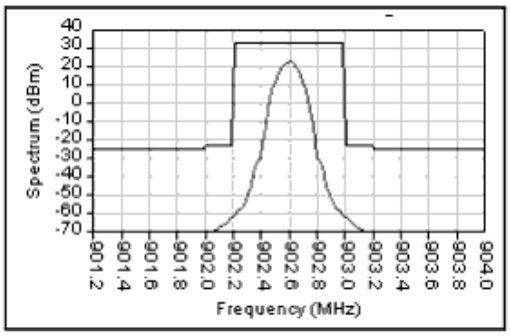
Only the data display template is provided in this workspace, but not simulation results because the dataset (MS_TxORFS_Step2.ds) is too large to be included in the package. To get the MS_TxORFS_Step2.ds and see the result curves, just run the designs MS_TxORFS_Step1 and then MS_TxORFS_Step2.

Test results shown in the following three figures are provided for reference, which are for the lowest (890.2 MHz), middle (902.6 MHz), and highest (914.8 MHz) frequencies.



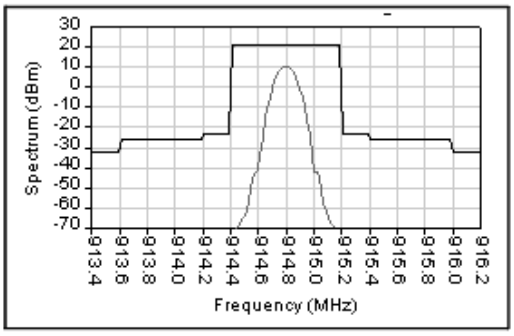
Output RF Spectrum, 890.2 MHz,

Power Level Set to 29 dBm



Output RF Spectrum, 902.6 MHz,

Power Level Set to 33 dBm



Output RF Spectrum, 914.8 MHz,

Power Level Set to 21 dBm

Benchmark

- Hardware platform: Pentium II 450 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3

- Data points: 100 time slots
- Simulation time: 30 minutes

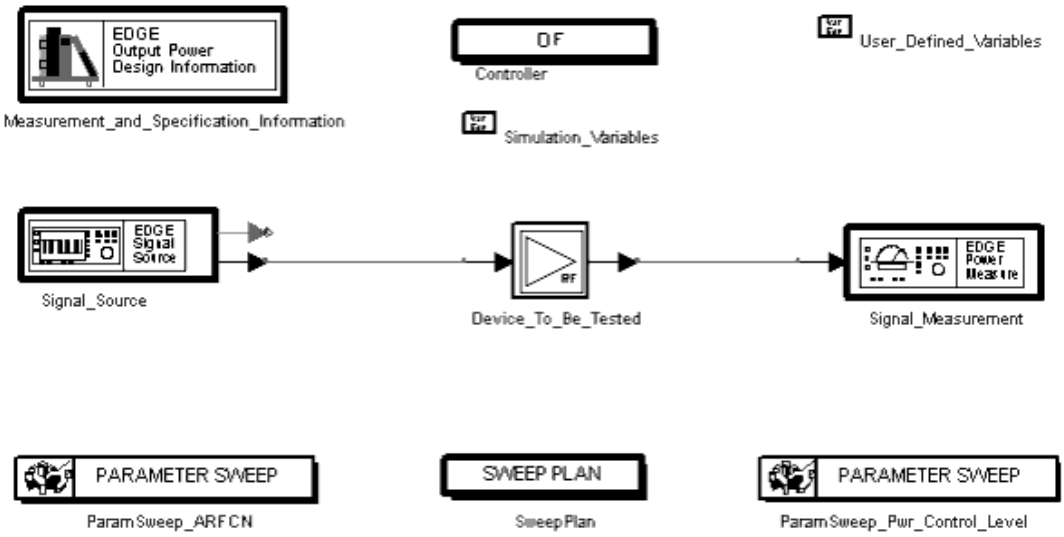
EDGE Power Amplifier Test Design Examples

Introduction

The EDGE_PA_Test_wrk provides design and verification solutions of power amplifier (PA) for EDGE wireless mobile station handsets. Six measurements are provided including error vector magnitude (EVM), frequency error and origin offset suppression (OOS), mean transmitted RF carrier power, transmitted RF carrier power versus time, output RF spectrum due to modulation and output RF spectrum due to switching.
Designs for these measurements are described in the following sections; they include:

- EVM measurements: EDGE_PA_MS_EVM
- frequency error and OOS measurements: EDGE_PA_MS_FreqErr_OffsetSupp
- mean transmitted RF carrier power measurements: EDGE_PA_MS_Power_Slope
- transmitted RF carrier power versus time measurements: EDGE_PA_MS_Power_vs_Time
- output RF spectrum due to modulation measurements: EDGE_PA_MS_RF_Spectrum_Mod
- output RF spectrum due to switching measurements: EDGE_PA_MS_RF_Spectrum_Switching

The following figure shows the top-level schematic for a typical power amplifier test design example.

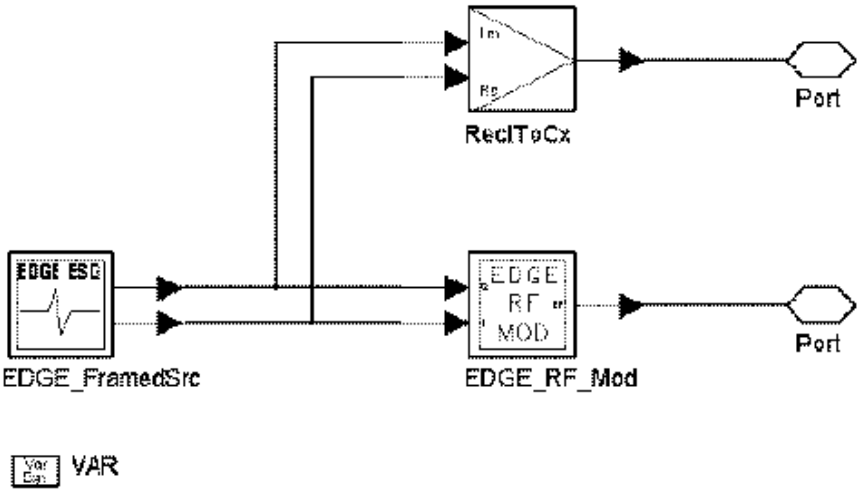


Top-Level Schematic of a Typical Design

A typical power amplifier design example includes these items.

- the _Information module contains measurement information and relevant industrial specification requirements.
- the DF (data flow) controller and VAR Simulation_Variables define control and simulation parameters. We recommend that designers do not modify the contents of these two components.
- the VAR User_Defined_Variables defines parameters for a specific measurement. Designers can customize these settings. Typical parameter settings are:
  - TS_Measured = 1

total of 8 time slots in one frame, numbered 0 to 7
    - SignalPower = dbmtow(33-DUT_Gain)
      Output signal power, after Device_To_Be_Tested, is set to 33 dBm which corresponds to 5, the power control level of the highest power for EDGE mobile stations.
    - RF_Freq = (890 + 0.2 × ARFCN) MHz
      Carrier frequencies are determined by ARFCN (absolute radio frequency channel number).
    - DUT_Gain = 25 (dB)
- ParamSweep_ARFCN and SweepPlan perform the parameter sweeps. For example, the FCarrier can be swept to make the measurement be implemented at the frequency points B((890 + 0.2 × 1) MHz), M((890 + 0.2 × 631) MHz) and T((890 + 0.2 × 124) MHz).
- the EDGE_Signal_Source module (schematic is shown in the following figure) generates the ESG Option 202 compatible RF band signals for measurement. It also generates complex reference signals, which are required in some measurements.
    - the output signal is in compliance with EDGE specifications, Release 1999, and therefore in compliance with Option 202 of ESG.
    - the eight time slots in one frame can be individually set to active or idle.
    - arbitrary output power can be set for the active time slots.



EDGE_Signal_Source Schematic

- the Device_To_Be_Tested module can be replaced by designer's power amplifier circuit. GainRF is used in the examples.
- the _Measurement subnetwork carries out the measurements.

Each design has a corresponding data display template which has the same file name as the design with a . *dds* extension. Power amplifier designers can use . *dds* data to display simulation results and do verifications of their own designs. Typically, . *dds* data consists of Main, Figures, and Equations pages.
A reference dataset of the simulation result of each example design can be found in the data directory, which has the extension of . *ds* and a prefix of *Ref_* .

Error Vector Magnitude Measurements

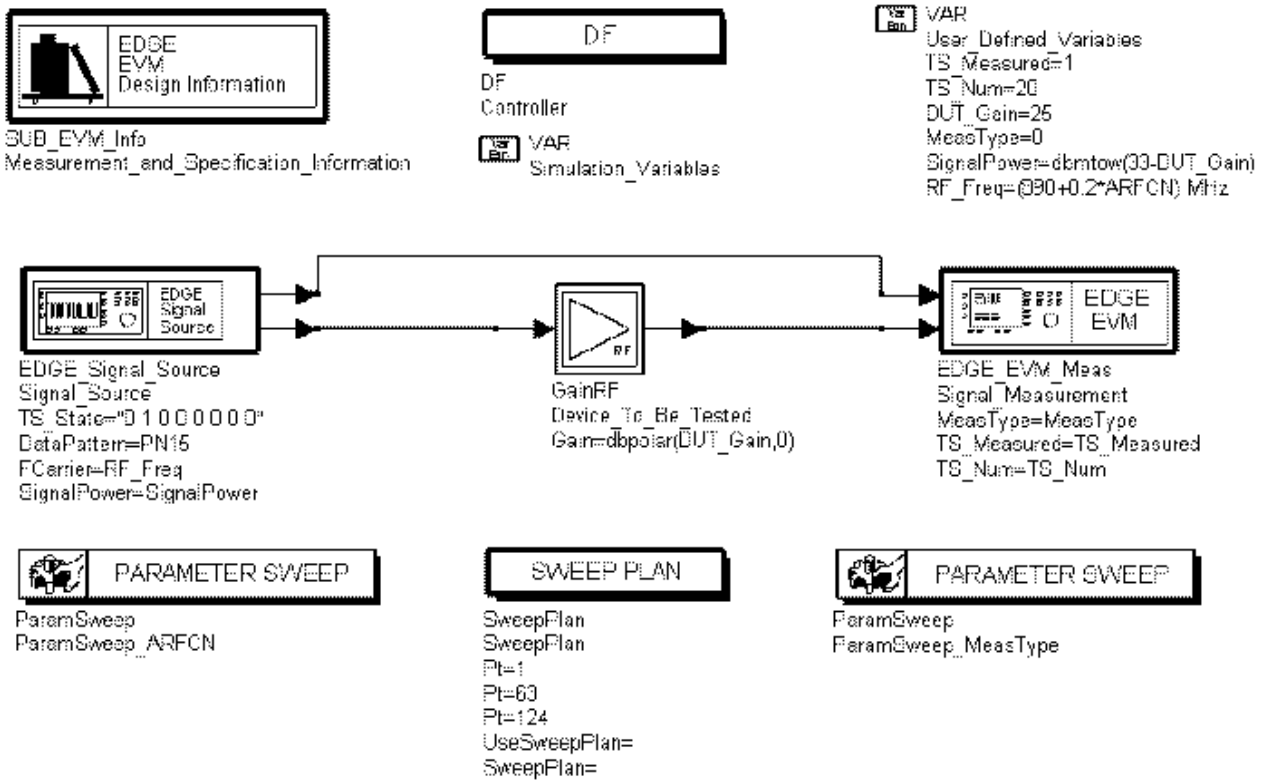
- EDGE_PA_MS_EVM Design

Description

For 8-PSK modulation, the error vector between the vector representing the transmitted signal and the vector representing the error-free modulated signal defines modulation accuracy. The magnitude of the error vector is called error vector magnitude (EVM).

This design is used to measure the RMS EVM, peak EVM and the 95th percentile EVM of the power amplifier at EGPRS mobile station transmitter then verify that they meet the industrial specifications. The test in this design is in compliance with the EDGE specifications Release 1999, therefore, it is in compliance with EVM measurements of Option 202 of ESG and VSA.

The top-level schematic for this design is shown in the following figure. The Measurement_and_Specification_Information subnetwork contains measurement information and industrial specifications. The Signal_Source subnetwork generates ESG Option 202 compatible RF band signal for measurement. The Signal_Measurement subnetwork implements the EVM measurements. In the Device_To_Be_Tested subnetwork, GainRF is used for demonstration.



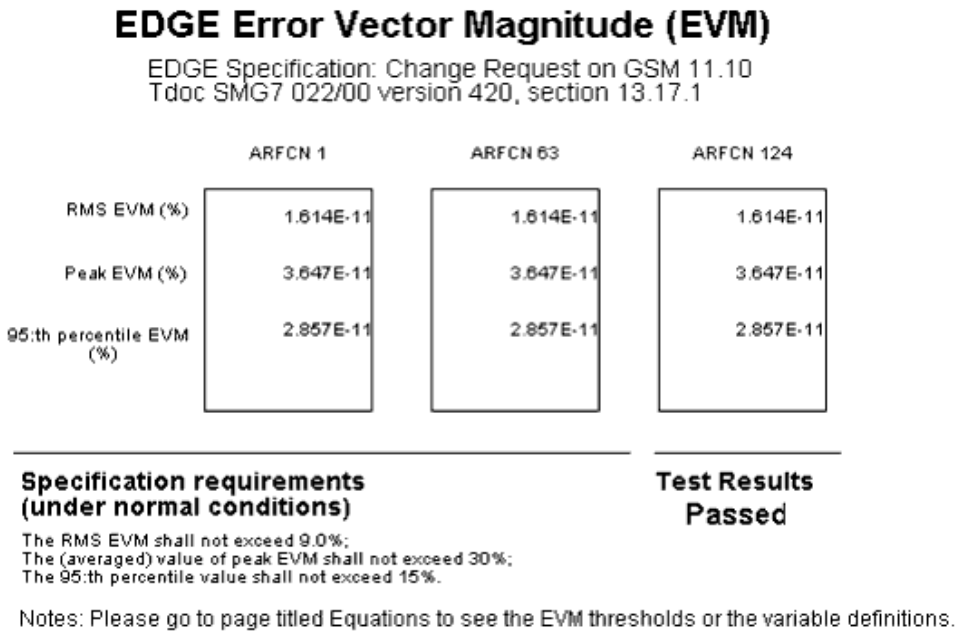
EDGE_PA_MS_EVM Schematic

Two sweeps are used to implement the three kinds of EVM measurements at the three frequency points required by industrial specifications. There are two data paths from the source to the measurement component. One is for the real transmitted signals which go through the device under test, and the other is for the reference signals needed in the measurement.

Output signal power after the Device_To_Be_Tested is set to 33 dBm, which corresponds to level 5, the power control level of the highest power for EDGE mobile stations. The variable TS_Num defines the number of time slots (bursts) that are averaged for the measurement. It should be at least 200 according to specification, but is set to 20 to reduce simulation time. Designers can set it in User_Defined_Variables.

Simulation Results

The simulation results are displayed in EDGE_PA_MS_EVM.dds, which consists of two pages: Main and Equations. Page Main contains the test results, that is the three EVMs at each of the three specified frequency points. It also contains the description of the specification requirements and the final results ("Passed" or "Failed") which indicates whether the test results meet the industrial specifications. Page Equations is for the equations that are used for the threshold definitions and the variable definitions and calculations. Page Main is shown in the following figure.



EDGE_PA_MS_EVM.dds

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 1.5
- Simulation Time: approximately 8 minutes

References

1. Tdoc SMG7 022/00 version 420, CR 11.10, section 13.17.1, Introduction of EGPRS Transmitter tests for frequency error, power, ORFS and intermodulation attenuation, March 22-24, 2000.
2. GSM 05.02, version 8.3.0, Release 1999.
3. GSM 05.05, version 8.3.0, Release 1999.

Frequency Error and Origin Offset Suppression Measurements

- EDGE_PA_MS_FreqErr_OffsetSupp Design

Description

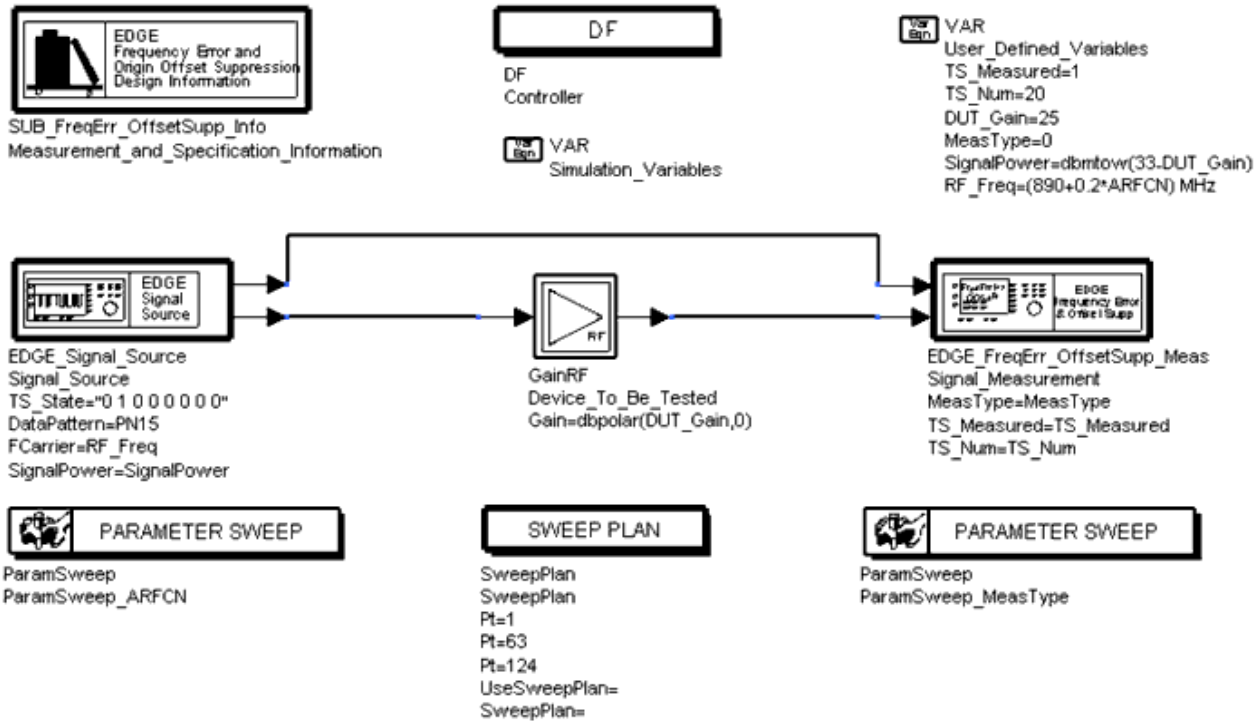
The frequency error is the difference in frequency, after adjustment for the effect of the modulation accuracy between the RF transmission from the mobile station and either the RF transmission from the base station or the nominal frequency for the ARFCN (absolute radio frequency channel number) used. The origin offset suppression (OOS) is a measurement of modulation accuracy, and is defined to be the ratio of the carrier leakage to the modulated signal.

This design is used to measure the frequency error and OOS of the power amplifier at EGPRS mobile station transmitter and then to verify that they meet the industrial specifications. The test in this design is in compliance with the EDGE specifications Release 1999, therefore, it is in compliance with the corresponding measurements of Option 202 of ESG and VSA.

The top-level schematic for this design is shown in the following figure. The Measurement_and_Specification_Information module contains measurement information and industrial specifications. The Signal_Source subnetwork generates ESG Option 202 compatible RF band signal for measurement. The Signal_Measurement subnetwork implements the measurements of frequency error or OOS.

In the Device_To_Be_Tested subnetwork GainRF is used as a demonstration. Two sweeps are used to implement the two kinds of measurements at the three frequency points that are required by industrial specifications. There are two data paths from the source to the measurement component. One is for the real transmitted signals which go through the device under test, and the other is for the reference signals needed in the measurement.

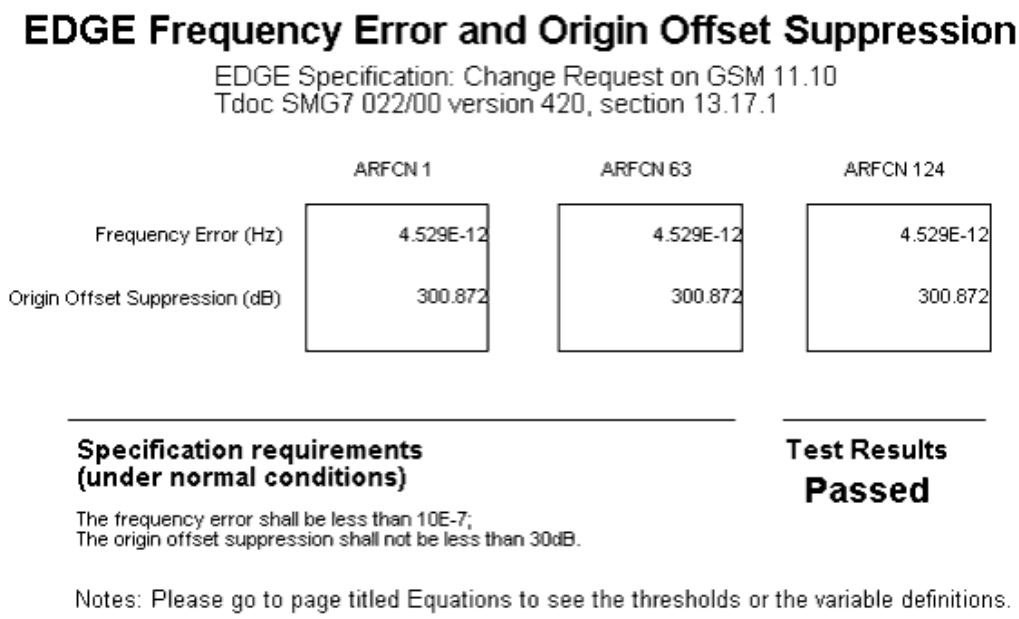
The output signal power after the Device_To_Be_Tested is set to 33 dBm, which corresponds to level 5, the power control level of the highest power for EDGE mobile stations. The variable TS_Num defines the number of time slots (bursts) that are averaged for the measurement. It should be at least 200 according to specification, but is set to 20 to reduce simulation time. Designers can set it in User_Defined_Variables.



EDGE_PA_MS_FreqErr_OffsetSupp Schematic

Simulation Results

The simulation results are displayed in EDGE_PA_MS_FreqErr_OffsetSupp.dds, which consists of two pages: Main and Equations. Page Main (see the following figure) contains the test results, that is the frequency error and OOS at each of the three specified frequency points. It also contains the description of the specification requirements and the final result ("Passed" or "Failed") which indicates whether the test results meet the industrial specifications. Page Equations is for the equations that are used for the threshold definitions and the variable definitions and calculations.



EDGE_PA_MS_FreqErr_OffsetSupp.dds

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 1.5
- Simulation Time: approximately 6 minutes

References

1. Tdoc SMG7 022/00 version 420, CR 11.10, section 13.17.1, Introduction of EGPRS Transmitter tests for frequency error, power, ORFS and intermodulation attenuation, March 22-24, 2000.
2. GSM 05.02, version 8.3.0, Release 1999.
3. GSM 05.05, version 8.3.0, Release 1999.

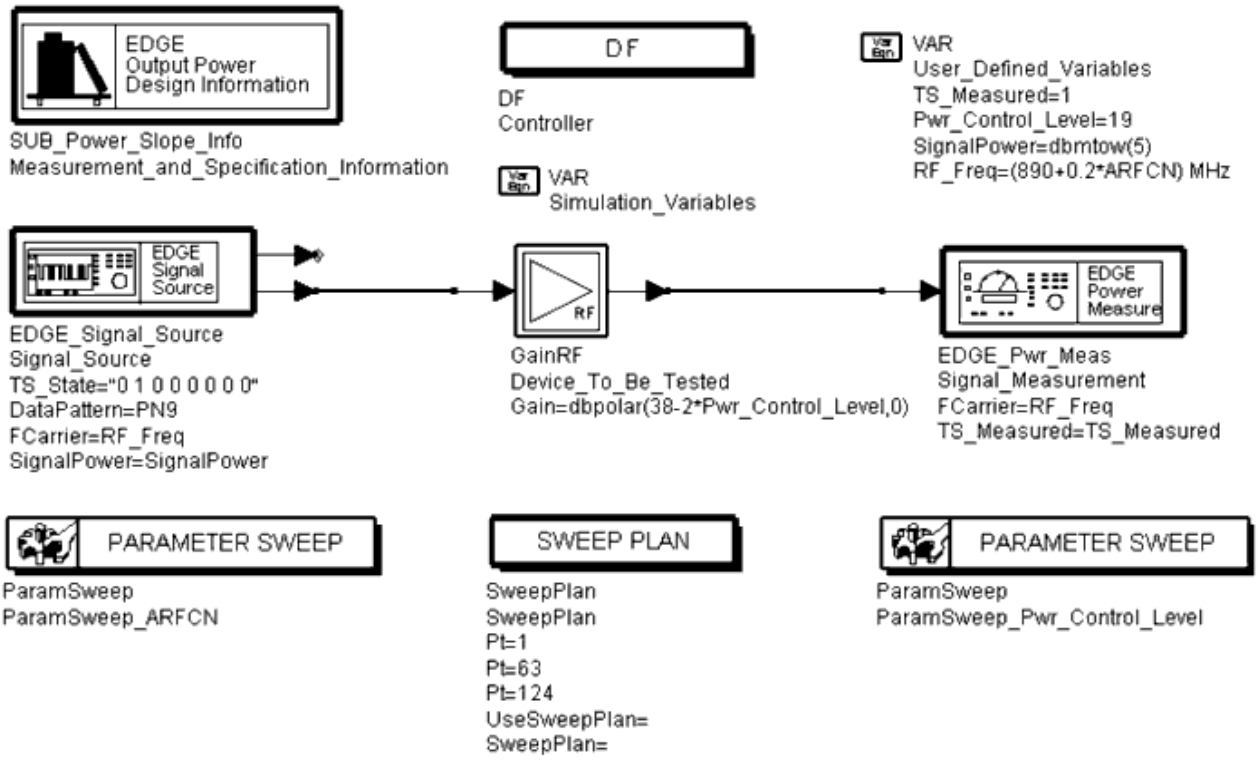
Mean Transmitter Output Power Measurement

- EDGE_PA_MS_Power_Slope Design

Description

Transmitter output power is the average value of power delivered to an artificial antenna or radiated by the mobile station and its integral antenna over the time that the useful information bits of one burst are transmitted.

The top-level schematic for this design is shown in the following figure. The SUB_Power_Slope_Info subnetwork contains measurement information and relevant industrial specifications. The EDGE_Signal_Source subnetwork generates RF signal for measurement. The EDGE_Pwr_Meas subnetwork implements mobile station transmitter output mean power measurements.



EDGE_PA_MS_Power_Slope

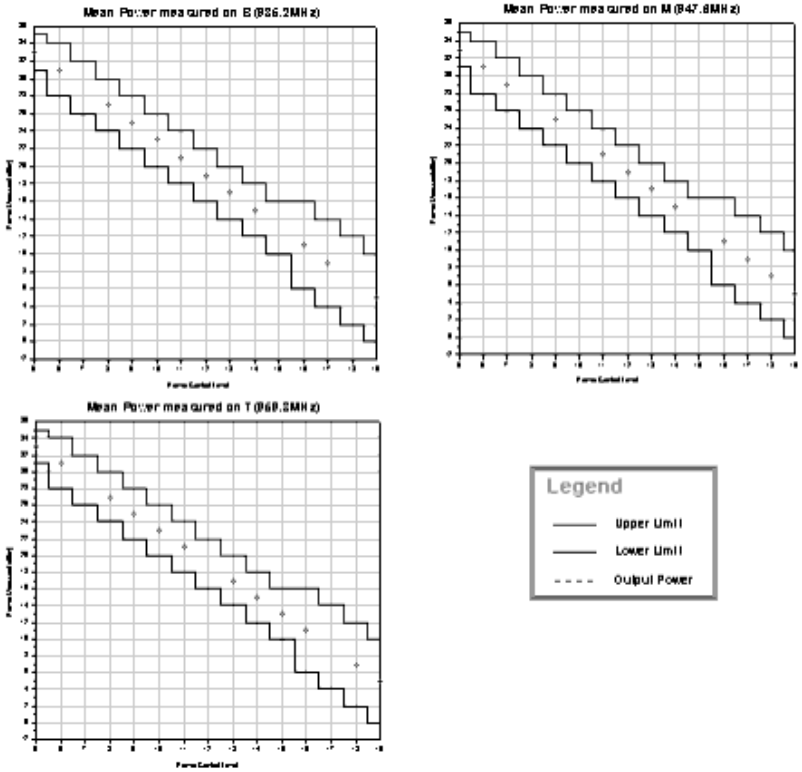
Simulation Results

Simulation results are displayed in EDGE_PA_MS_Power_Slope.dds, which consists of three pages: Main, Figures and Equations. Page Main (see the first of the following two figures) contains the most important results. Page Figures (see the second figure) shows the results of power slope. Page Equations contains all variable definitions and

calculations.

Specification Requirement			Test Results
Power Control Level	Transmitter Output Power	Tolerances (Normal)	
5	33	+/- 2 dB	Passed
6	31	+/- 3 dB	
7	29	+/- 3 dB	
8	27	+/- 3 dB	
9	25	+/- 3 dB	
10	23	+/- 3 dB	
11	21	+/- 3 dB	
12	19	+/- 3 dB	
13	17	+/- 3 dB	
14	15	+/- 3 dB	
15	13	+/- 3 dB	
16	11	+/- 5 dB	
17	9	+/- 5 dB	
18	7	+/- 5 dB	
19	5	+/- 5 dB	

EDGE_PA_MS_Power_Slope Simulation Results



EDGE_PA_MS_Power_Slope Simulation Results Data Display

Benchmark

- Hardware Platform: Pentium III 1000 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, ADS 1.5
- Simulation Time: approximately 85 minutes

References

1. ETSI Tdoc SMG7 022/00 version 420, CR 11.10, section 13.17.3, Introduction of EGPRS Transmitter tests for frequency error, power, ORFS and intermodulation attenuation, March 22-24, 2000.
2. GSM 05.02, version 8.3.0, Release 1999.
3. GSM 05.05, version 8.3.0, Release 1999.

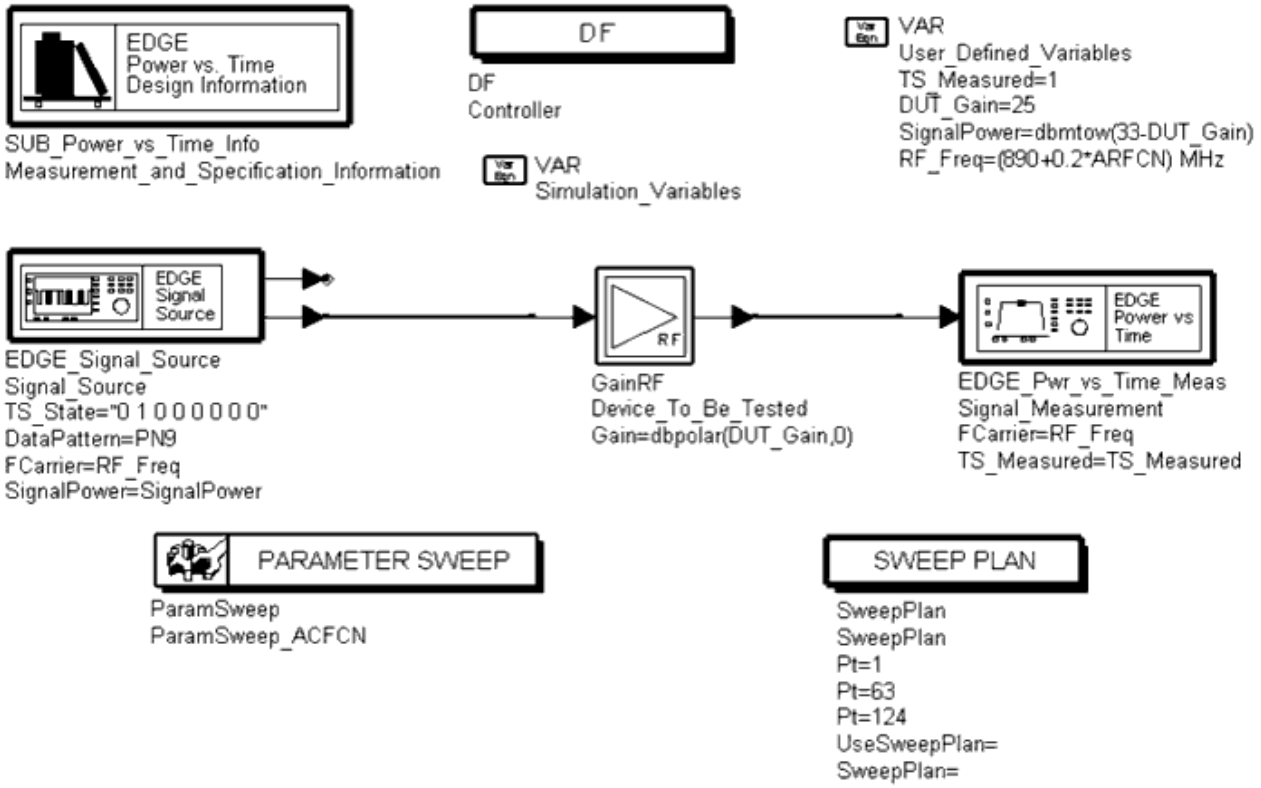
Transmitted RF Carrier Power versus Time Measurement

- EDGE_PA_MS_Power_vs_Time Design

Description

This design measures the mean transmit power during the *useful part* of EDGE bursts and verifies that the power ramp fits within the defined mask. This design also shows the rise, fall, and *useful part* of the EDGE burst.

The top-level schematic for this design is shown in the following figure. The SUB_Power_vs_Time_Info subnetwork contains measurement information and relevant technical specifications. The EDGE_Signal_Source subnetwork generates RF signal for measurement. The EDGE_Pwr_vs_Time_Meas subnetwork implements mobile station transmitter output power versus time measurement.



EDGE_PA_MS_Power_vs_Time

Simulation Results

Simulation results are displayed in EDGE_PA_MS_Power_vs_Time.dds, which consists of three pages: Main, Figures and Equations. Page Main (see the first of the following two

figures), contains the most important results. Page Figures (see the second figure), shows the power versus time curves. Page Equations contains all variable definitions and calculations

EDGE Mobile StationTransmitted RF Carrier Power versus Time

EDGE Specification: Change Request on GSM 11.10
Tdoc SMG7 022/00 version 420, section 13.17.3

Specification Requirement

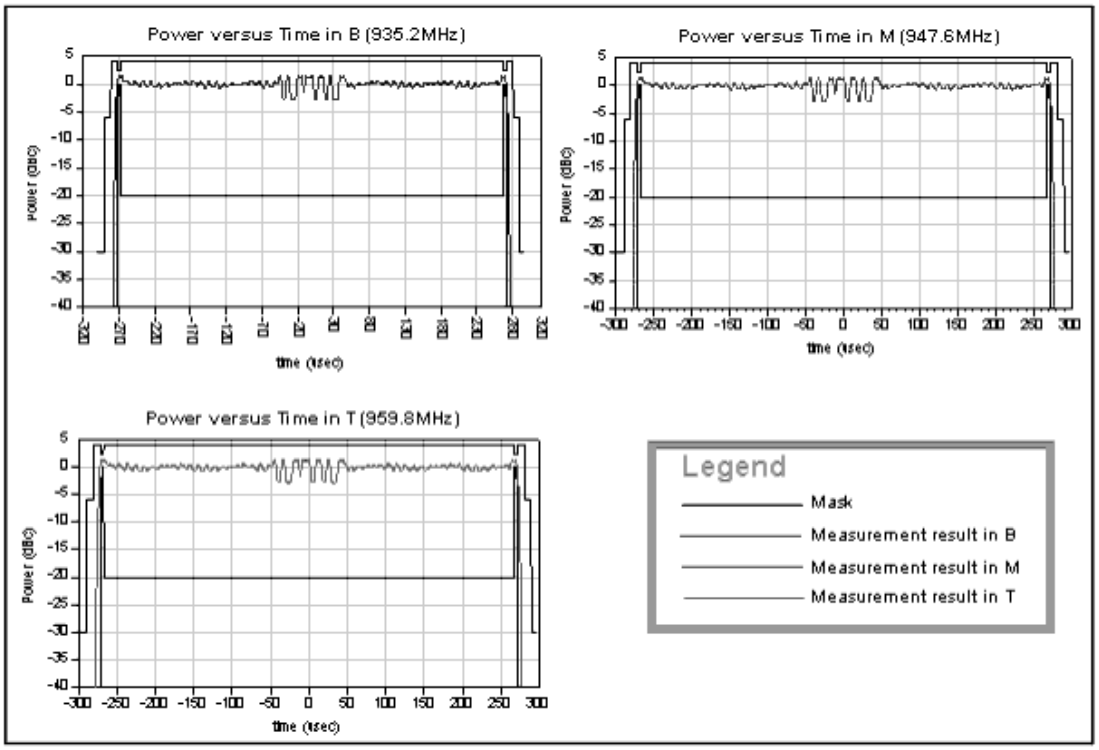
Please see mask definitions in page titled Equations.
The test result curves should be within the masks.

Test Results

Test **Passed** if the curve of power vs time doesn't exceed the mask.
Otherwise, test **Failed** .

Notes: Please go to page titled Equations to see the masks and the variable definitions.
Please go to page titled Figures to see the result curves with the masks.

EDGE_PA_MS_Power_vs_Time Simulation Results



EDGE_PA_MS_Power_vs_Time Simulation Results Data Display

Benchmark

- Hardware Platform: Pentium III 1000 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, ADS 1.5
- Simulation Time: approximately 3 minutes

References

1. ETSI Tdoc SMG7 022/00 version 420, CR 11.10, section 13.17.3, Introduction of EGPRS Transmitter tests for frequency error, power, ORFS and intermodulation attenuation, March 22-24, 2000.
2. GSM 05.02, version 8.3.0, Release 1999.
3. GSM 05.05, version 8.3.0, Release 1999.

Output RF Spectrum due to Modulation Measurement

- EDGE_PA_MS_RF_Spectrum_Mod Design

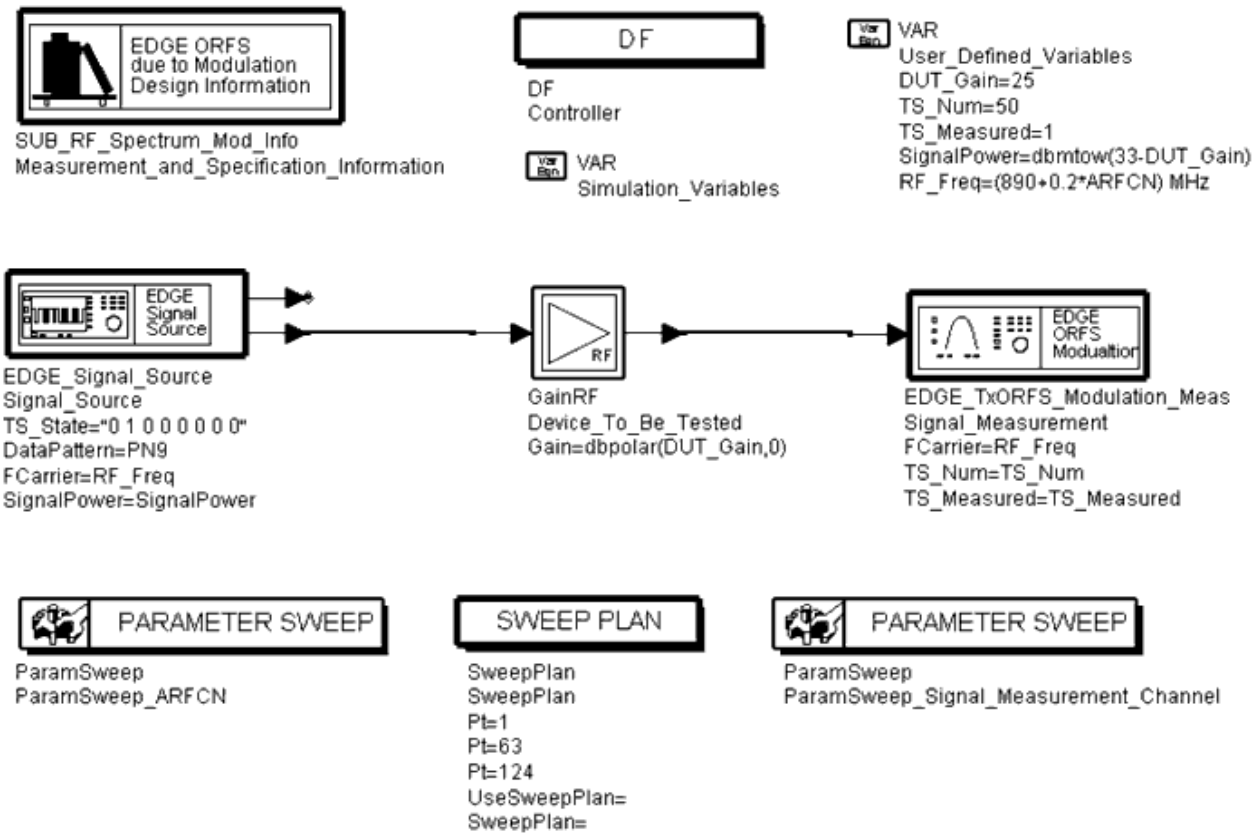
Description

The output RF spectrum due to modulation is the relationship between the frequency offset from the carrier and the power, measured in a specified bandwidth and time, produced by the mobile station due to the effect of modulation.

The measurement provides information about distribution of the mobile station transmitter out-of-channel spectral energy due to modulation.

The top-level schematic for this design is shown in the following figure. The SUB_RF_Spectrum_Mod_Info subnetwork contains measurement information and relevant industrial specifications. The EDGE_Signal_Source subnetwork generates RF and signal for measurement.

The EDGE_TxORFS_Modulation_Meas subnetwork implements ORFS due to modulation measurement. In this measurement, a 30 kHz bandwidth, 5-pole synchronously tuned filter is used. The sweep range is -600 kHz to 600 kHz.



EDGE_PA_MS_RF_Spectrum_Mod

Simulation Results

Simulation results are displayed in EDGE_PA_MS_RF_Spectrum_Mod.dds, which consists of three pages: Main, Figures and Equations. Page Main (see the first of the following two figures) contains the most important final results and indicates if the measurement results meet the requirements of industrial specification. Page Figures (see the second figure) shows the ORFS due to modulation. Page Equations contains all variable definitions and calculations.

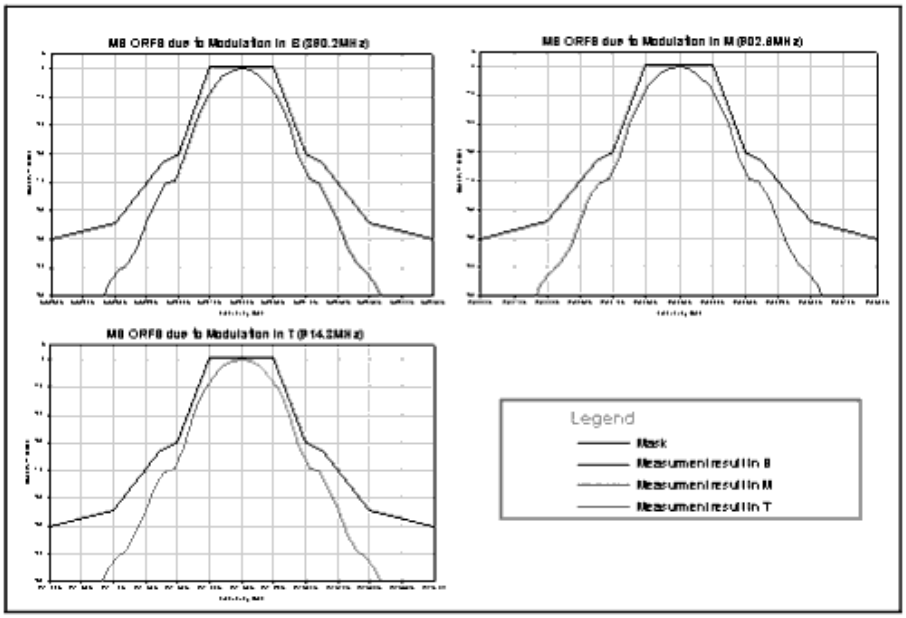
Specification Requirement

Power level (dBm)	Power levels in dB relative to the measurement at RF channel nominal center frequency Frequency offset (kHz)							
	0-100	200	250	400	600 to 1800	1800 to 3000	3000 to 6000	>=6000
<=33	0.5	-30	-33	-54	-60	-63	-65	-71

Test Results

Test Passed if the curve of RF Spectrum due to modulation doesn't exceed the mask.
Otherwise, test Failed .

EDGE_PA_MS_RF_Spectrum_Mod Simulation Results



EDGE_PA_MS_RF_Spectrum_Mod Simulation Results Data Display

Benchmark

- Hardware Platform: Pentium III 1000 MHz, 512 MB memory
- Software Platform: Windows 2000 Workstation, ADS 1.5
- Simulation Time: 252 minutes

References

1. Tdoc SMG7 022/00 version 420, CR 11.10, section 13.17.4, Introduction of EGPRS Transmitter tests for frequency error, power, ORFS and intermodulation attenuation, March 22-24, 2000.
2. GSM 05.02, version 8.3.0, Release 1999.
3. GSM 05.05, version 8.3.0, Release 1999.

Output RF Spectrum due to Switching Measurement

EDGE_PA_MS_RF_Spectrum_Switching Design

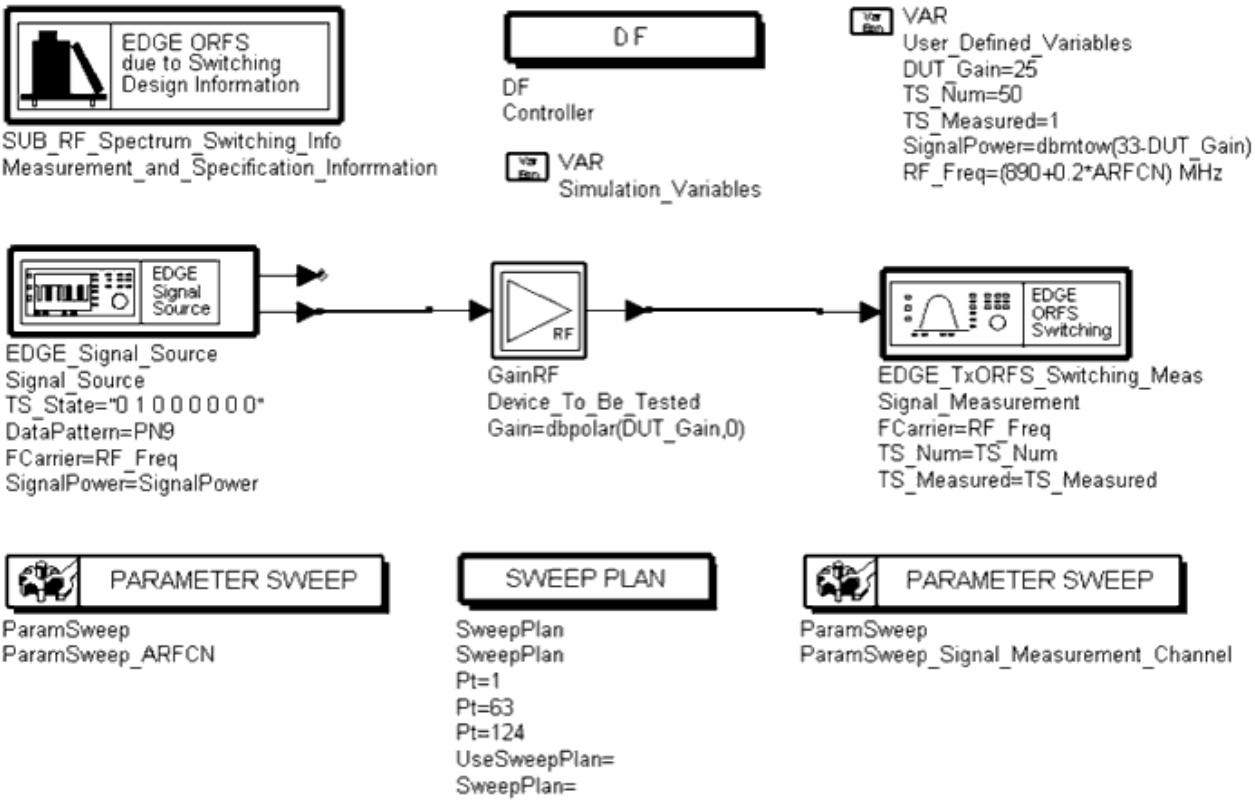
Description

The output RF spectrum due to switching is the relationship between the frequency offset from the carrier and the power, measured in a specified bandwidth and time, produced by the mobile station due to the effect of power ramping.

The measurement provides information about distribution of the mobile station transmitter's out-of-channel spectral energy due to switching.

The top-level schematic for this design is shown in the following figure. The SUB_RF_Spectrum_Switching_Info subnetwork contains measurement information and relevant industrial specifications.The EDGE_Signal_Source subnetwork generates the RF signal for measurement.

The EDGE_TxORFS_Switching_Meas subnetwork implements ORFS due to switching measurement. In this measurement, a 30 kHz bandwidth, 5-pole synchronously tuned filter is used. The sweep range is -600 kHz to 600 kHz.



EDGE_PA_MS_RF_Spectrum_Switching

Simulation Results

Simulation results are displayed in EDGE_PA_MS_RF_Spectrum_Switching.dds, which consists of three pages: Main, Figures and Equations. Page Main (see the first of the following two figures) contains the most important final results and indicates if the measurement results meet the requirements of industrial specification.

The second figure shows the Figures page. However, the result curves of the simulation are not displayed in that page, only data display template is provided. This is because that the result dataset (EDGE_PA_MS_RF_Spectrum_Switching.ds) is not provided in EDGE package for the sake of package size. To get the EDGE_PA_MS_RF_Spectrum_Switching.ds and see the result curves, just run the design EDGE_PA_MS_RF_Spectrum_Switching. Page Equations contains all variable definitions and calculations.

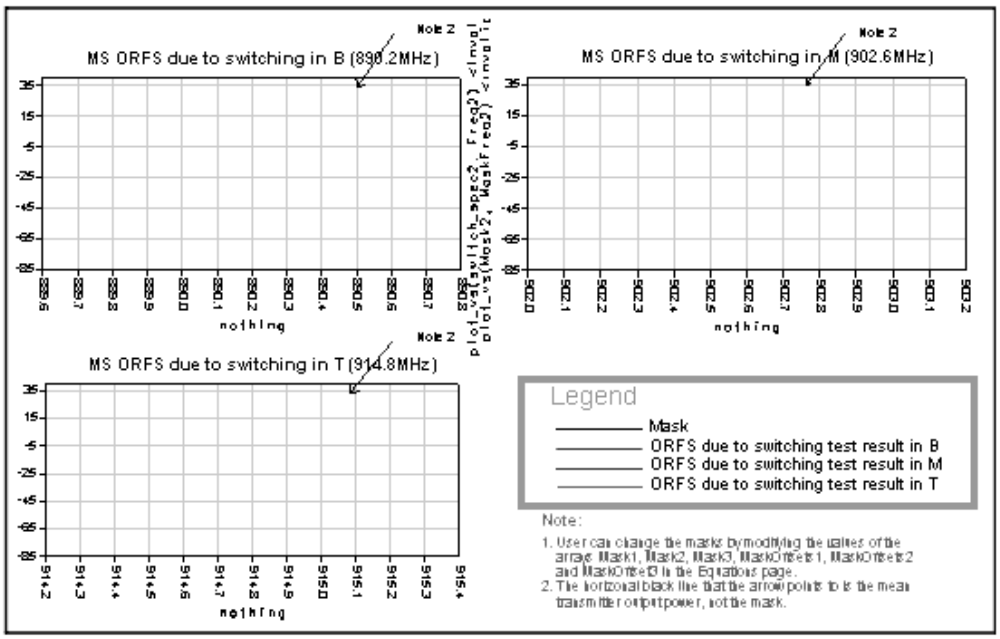
Specification Requirement

Power level	Maximum level for various offsets from carrier frequency			
	400 kHz	600 kHz	1200 kHz	1800 kHz
33 dBm	-19 dBm	-21 dBm	-21 dBm	-24 dBm

Test Resuls

Test **Passed** if the curve of RF Spectrum due to switching doesn't exceed the mask. Otherwise, test **Failed** .

EDGE_PA_MS_RF_Spectrum_Switching Simulation Results



EDGE_PA_MS_RF_Spectrum_Switching Simulation Results Data Display (arrows point to mean transmitted power, not masks)

Benchmark

- Hardware Platform: Pentium III 1000 MHz, 512 MB memory
- Software Platform: Windows 2000 Workstation, ADS 1.5
- Simulation Time: approximately 255 minutes

References

1. Tdoc SMG7 022/00 version 420, CR 11.10, section 13.17.4, Introduction of EGPRS Transmitter tests for frequency error, power, ORFS and intermodulation attenuation, March 22-24, 2000.
2. GSM 05.02, version 8.3.0, Release 1999.
3. GSM 05.05, version 8.3.0, Release 1999.

EDGE Signal Source Design Examples

Introduction

The EDGE_Signal_Source_wrk workspace is part of the EDGE Test & Verification Library package and is based on the ESG uplink and downlink EDGE signal generation features.

Design examples include:

- Patterned and modulated baseband signal measurements: SS_PatternedSrc and EDGE_PatternedSrc
- Framed and modulated baseband signal measurements: SS_FramedSrc and EDGE_FramedSrc

Designs in this workspace consist of:

- EDGE_EVM_WithRef is used to measure the RMS EVM
- EDGE_Pwr_Measure is used to measure the mean transmitted power
- SpecAnalyzer is used to measure the transmitted power spectrum
- transmission modulation and up-converter: data from the baseband signal source for EDGE is up-converted to a 71 MHz RF signal with EDGE_RF_Mod, then modulated into a 935 MHz RF signal with EDGE_RF_TX_IFin.

Patterned and Modulated Baseband Signal Measurements

EDGE_Signal_Source_wrk Design Names

- SS_PatternedSrc
- EDGE_PatternedSrc

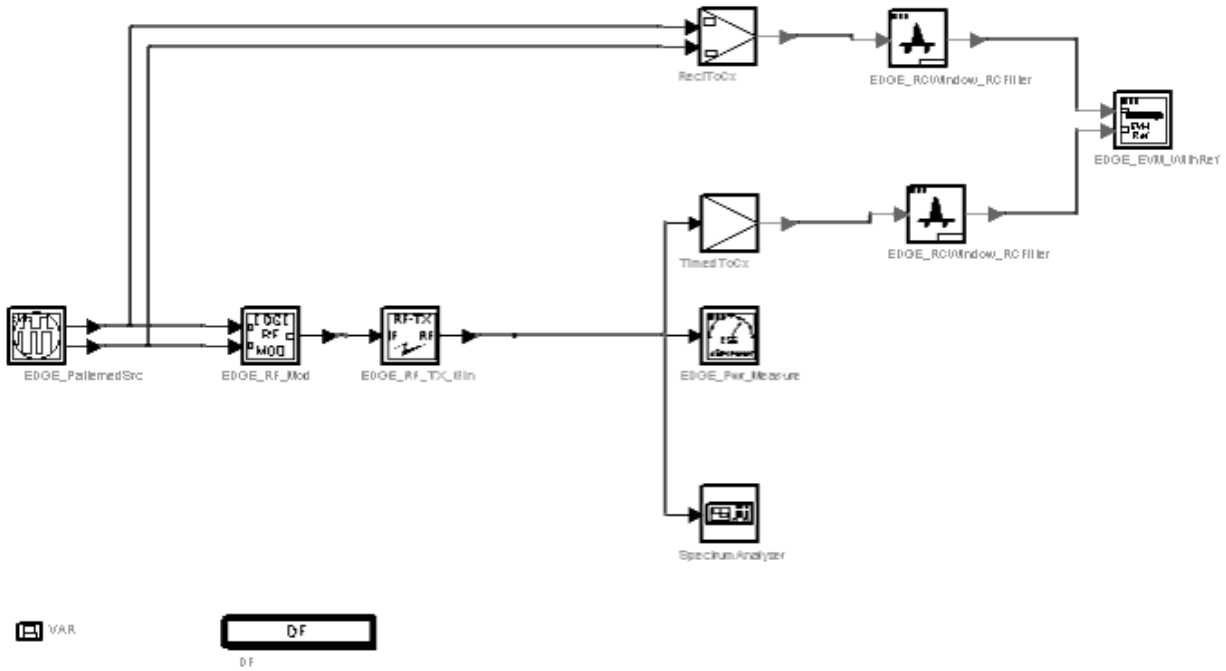
Features

- RMS EVM, mean transmitted power and transmitted power spectrum measurements
- integrated RF section
- adjustable sample rate

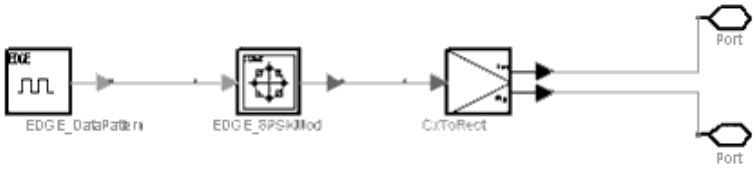
Description

SS_PatternedSrc is used to measure the RMS EVM, mean transmitted power and transmitted power spectrum of EDGE_PatternedSrc. The schematic for this design is shown in the first of the following two figures.

EDGE_PatternedSrc can generate one of eight patterned and modulated baseband signals without frame structure. The schematic for this design is shown in the second figure.



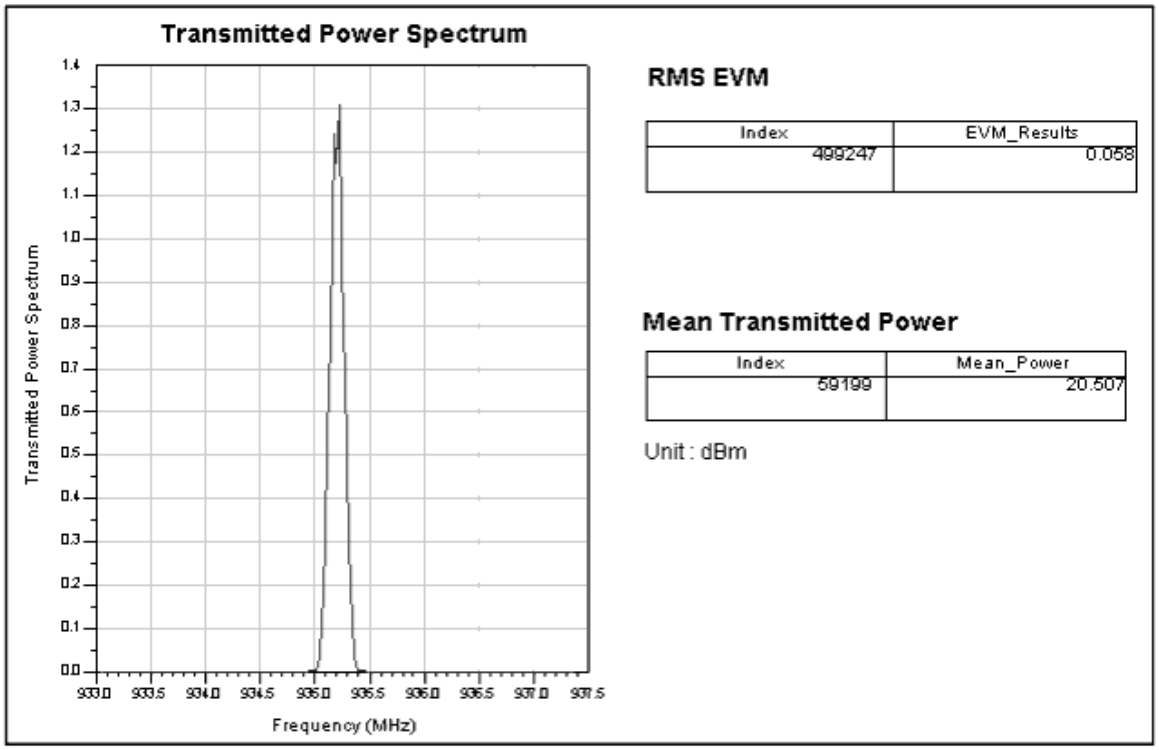
SS_PatternedSrc Schematic



EDGE_PatternedSrc Schematic

Test Results

Test results are shown in the following figure.



SS_Patterned_Src.dds Test Results

Benchmark

- Hardware platform: Pentium II 800 MHz, 512 MB memory
- Software platform: Windows NT 4.0 Workstation, ADS 1.3
- Time slots to be averaged: 200 time slots
- Simulation Time: approximately 6 minutes

Framed and Modulated Baseband Signal Measurements

EDGE_Signal_Source_wrk Design Name

- SS_FramedSrc
- EDGE_FramedSrc

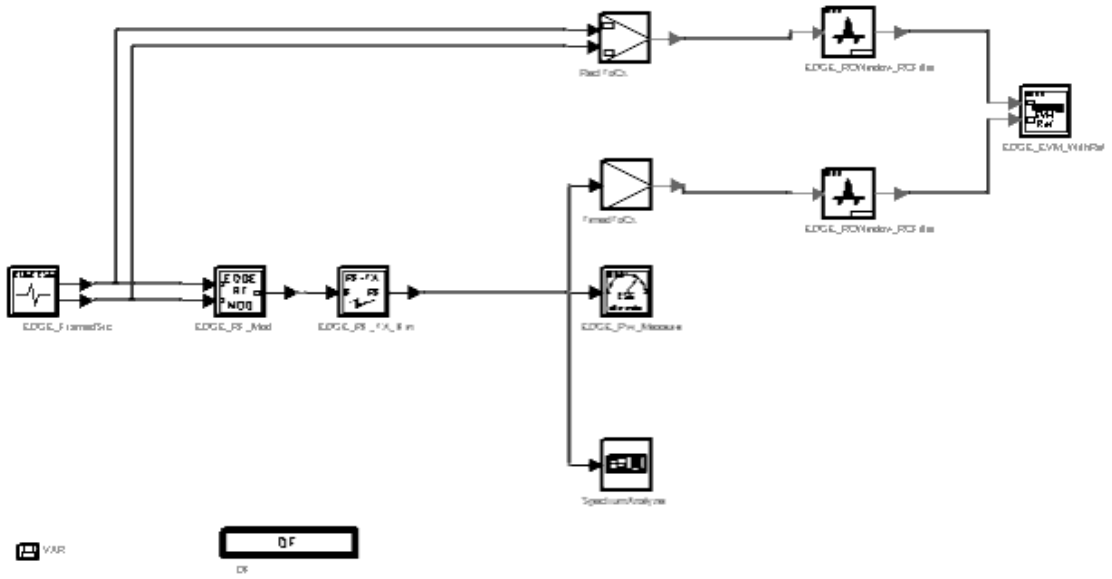
Features

- RMS EVM, mean transmitted power and transmitted power spectrum measured
- RF section integrated
- Sample rate adjustable

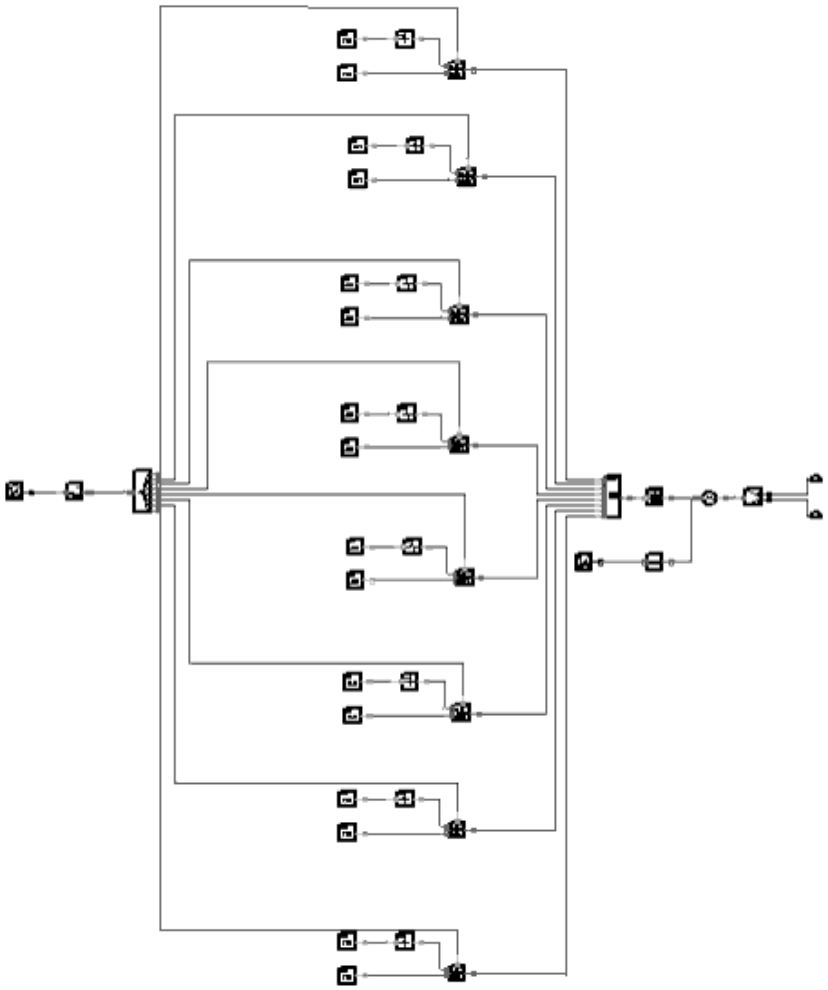
Description

SS_FramedSrc is used to measure the RMS EVM, mean transmitted power and transmitted power spectrum of EDGE_FramedSrc. The schematic for this design is shown in the first of the following two figures.

EDGE_FramedSrc can generate one of eight patterned and modulated baseband signals with frame structure. The schematic for this design is shown in the second figure.



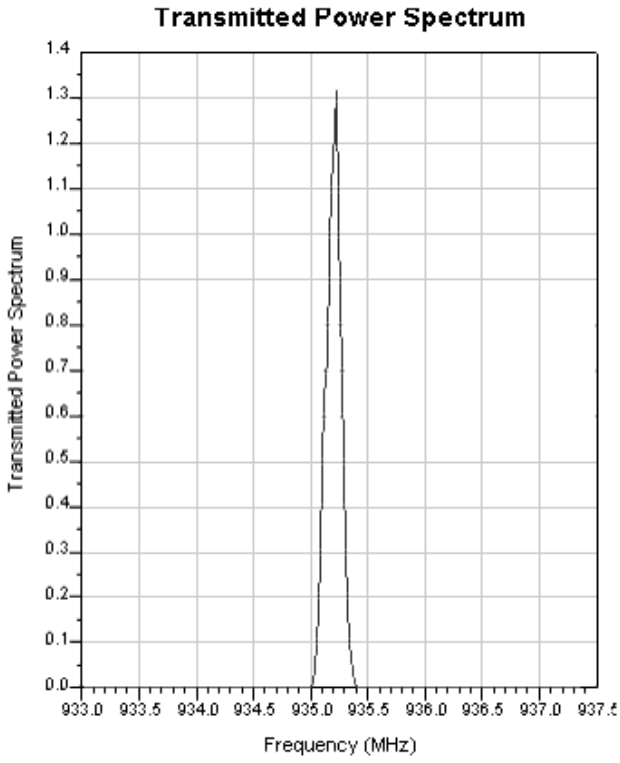
SS_FramedSrc Schematic



EDGE_FramedSrc Schematic

Test Results

Test results are shown in the following figure.



EVM RMS

Index	EVM_Results
499247	0.064

Mean Transmitted Power

Index	Mean_Power
59199	20.370

Unit : dBm

SS_Framed_Src.dds Test Results

Benchmark

- Hardware Platform: Pentium II 800 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, ADS 1.3
- Time slots to be averaged: 200 time slots
- Simulation Time: approximately 6.5 minutes

Equalization Components for EDGE Design Library

- *EDGE ChannelEstimator* (edge)
- *EDGE DeRotator* (edge)
- *EDGE Equalizer* (edge)
- *EDGE EqualizerAB* (edge)
- *EDGE EquCombiner* (edge)
- *EDGE EquComposeAB* (edge)
- *EDGE EquDeComposeAB* (edge)
- *EDGE EquSplitter* (edge)
- *EDGE EquStateToFloat* (edge)
- *EDGE MatchedFilter* (edge)
- *EDGE VAProcessor* (edge)

EDGE_ChannelEstimator

Description Channel estimator
Library EDGE, Equalization
Class SDFEDGE_ChannelEstimator

Parameters

Name	Description	Default	Sym	Type	Range
Direction	direction of estimation: Forward, Backward	Forward		enum	
BurstType	burst type: Normal Burst, Synchronization Burst, Access Burst	Normal Burst		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]

Pin Inputs

Pin	Name	Description	Signal Type
1	input	synchronized and derotated data	complex
2	tssi	training sequence selection indicator: TSC for normal burst; 0 to 2 for access burst; ignored for synchronization burst	int

Pin Outputs

Pin	Name	Description	Signal Type
3	output	complex channel impluse response estimate	complex
4	index	index to correct synchronization	int

Notes/Equations

1. This model is used to estimate the impulse response of the equivalent channel which includes the effect of modulation and de-rotation. L+1 output tokens are produced at pin output and one token is produced at pin index for each N input tokens consumed at pin input and one token consumed at pin tssi; refer to the following table for N values.

BurstType	N
Normal Burst	87 + 2×L
Synchronization Burst	106 + 2×L
Access Burst	80 + 2×L

2. This model provides either forward or backward directional channel estimation in each burst period. It's known that the central 16 symbols of the EDGE training sequence have good autocorrelation properties with low main to side lobe ratio. Also the five symbols on both sides are quasi-periodically repeated symbols. In every burst, the model correlates the training sequence in received data from pin input with the same known sequence which is selected by the input from pin tssi, estimates the CIR (channel impulse response) coefficients and sends to pin output. Also, the model uses a sliding window to further calibrate synchronization and send resulting index for calibration from pin index. Both the CIR and the index will aid the Viterbi processor in equalization.
3. Define the reference training sequence as p_i, i = 0, 1, ... , 25, then any item $p_k \in \{\pm 1\}$. Let y_n be the central training sequence part of the input data, $n = n\ 0+5$, $n\ 0+6$, ... , $n\ 0+20$, where $n\ 0$ is the index of the first bit of training sequence in received data. And define the estimate of the channel coefficients h'_l as $h'0$, $h'1$, ... , h'_L, where L is the value of parameter MaxDelay. Then, in practice are the following properties and relations:

$$\frac{1}{16}\sum_{5}^{20} p_k^2 = 1,$$

$$\frac{1}{16}\sum_{5}^{20} p_k p_{k-l} \approx 0, |l| \le 6.$$

Assume the real channel coefficient is hl,while the estimate is h'l. To get the estimate, {yn} first correlates with the reference training sequence {pn}, to estimate long enough hl, then truncate continuous L coefficients of the estimation which have the maximum energy, to set as h'l, l = 0, 1, ... , L. That is:

$$\hat{h}_l = \sum_{k=5}^{2} y_{k+n_0} p_{k-l}, \quad l = -5, -4, ..., 5,$$

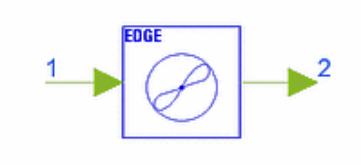
$$h'_l \mid 0 \le l \le 5\} = max(\{\hat{h}_{m+l} \mid 0 \le l \le 5\})$$

where the maximum is taken over all the possible m ($-5 \le m \le 0$).

References

1. R. Steele, Mobile Radio Communications. London: Pentech Press, 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 4.8.0, Nov. 1996.
3. Tdoc SMG2 EDGE 2E99-403, New Training Sequences for Access Burst due to EGPRS, August 24 -27, 1999

EDGE_DeRotator



Description De-rotator
Library EDGE, Equalization
Class SDFEDGE_DeRotator

Parameters

Name	Description	Default	Type
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input data sequence	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output data sequence	complex

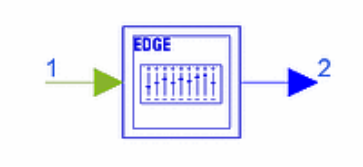
Notes/Equations

1. This model is used to de-rotate the received signals to compensate for the rotation introduced by Modified 8PSK or GMSK modulation.
   156 output tokens are produced for each 156 input tokens consumed at input.
2. GMSK modulation introduces a rotation in the signal phase: the π/2 increase or decrease of the phase in each bit duration. Similarly, a consecutive phase rotation of 3/8 π is introduced when modified 8PSK modulation is used. Removing this phase rotation before the matched filter will simplify the successive processes.

References

1. ETSI Tdoc SMG2 WPB 108/98, Ericsson, EDGE Evaluation of 8-PSK.

EDGE_Equalizer



Description Adaptive equalizer for normal and synchronization bursts
Library EDGE, Equalization
Class SDFEDGE_Equalizer

Parameters

Name	Description	Default	Sym	Type	Range
BurstType	burst type: Normal Burst, Synchronization Burst	Normal Burst		enum	
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK		enum	
TSC	training sequence code	0		int	[0, 7]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†
† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$					

Pin Inputs

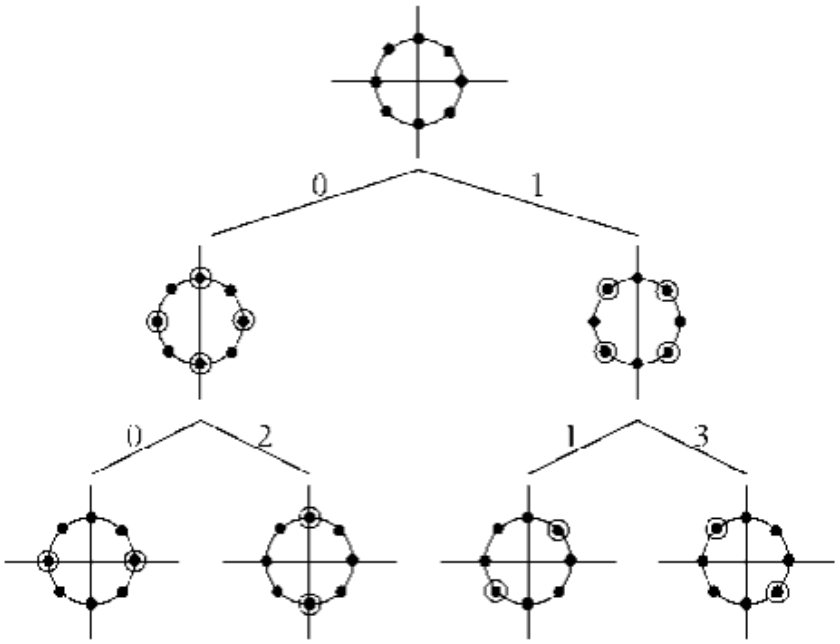
Pin	Name	Description	Signal Type
1	input	synchronized signal to be equalized	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	output	bit sequence after equalization	real

Notes/Equations

1. This subnetwork is the adaptive equalizer in EDGE receiver, which is used to restore the data sequence from the received and synchronized signals.
   It is known that the maximum-likelihood sequence estimation (MLSE) equalizer is the optimum receiver for channels with ISI, which is caused by channel distortion, and additive white Gaussian noise (AWGN). However, in general, the implementation complexity of MLSE implemented with the Viterbi algorithm (VA) is roughly M^K times that of a decision-feedback equalizer (DFE), where K is the length of the overall channel impulse response and M is the size of the signal set.
   Preprocessing techniques can be employed to reduce the channel response to a shorter length. In the systems like EDGE which use large signal set (M, M=8 in EDGE for 8PSK) the complexity still can be high even for very small K. For example, in the MLSE implementation for EDGE, if K is reduced to 5 with M=8, the VA will search a (ML) trellis with M^K ($= 8^5 = 32768$) states, and therefore has to keep track of the 8^5 paths.
   Reduced-state sequence estimation (RSSE) is employed to lower the complexity. The EDGE_VAProcessor subnetwork can achieve nearly the performance of MLSE at significantly reduced complexity. The primary idea is the construction of trellis with a reduced number of states. These states are formed by combining the states of the ML trellis using Ungerboeck-like set partitioning principles. The RSSE is then implemented using the VA to search this reduced-states trellis.
   The following figure demonstrates the Ungerboeck-like set partition for 8PSK modulation.

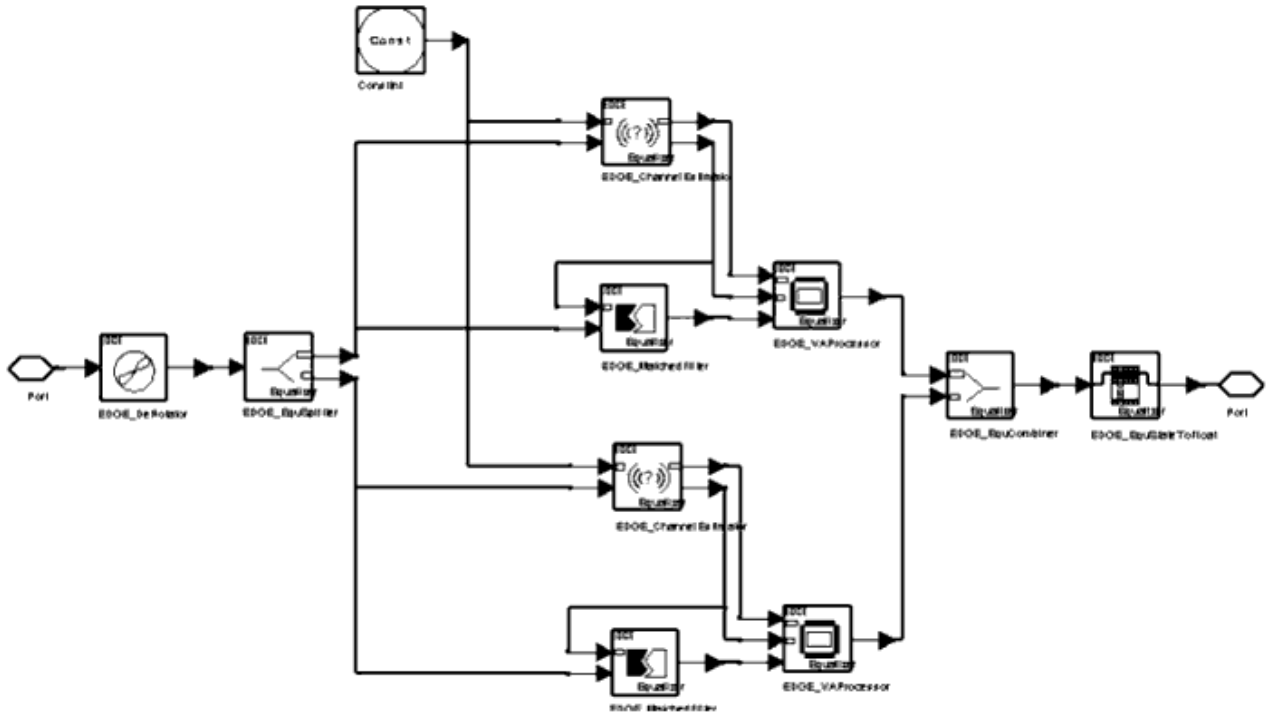


The root of the tree represents the 8-point signal set being combined into one subset. The branches under it denote the set partitions of two and four subsets (eight subsets means no partitioning).
In EDGE, since L is limited to 5, the ML trellis states may be denoted as a vector of 5 elements $[x_1, x_2, x_3, x_4, x_5]$ (!edge-05-04-16.gif! is the most recent transmitted symbol), each of which may have M=8 values. After the partitioning, the signal set is partitioned into J_k subsets for each x_k ($1 \le k \le 5$, $1 \le J_k \le 8$). Thus the state number is largely reduced.

The partitioning scheme may be denoted by J_k as J_1, J_2, J_3, J_4, J_5, where J_1 corresponds to the most recent transmitted symbol. And, three constraints are added:

- the numbers J_k are nonincreasing (i.e., !edge-05-04-25.gif!);
- the partition of x_{k+1} is a further partition of the subsets of x_k;
- J_k is a power of two (for good performance). The vector or array J_1, J_2, J_3, J_4, J_5 is called the partition array.
  The parameter PartitionArray gives the way to define the partition. It determines the implementation and computational complexity of the RSSE equalizer. For example, if the partition array is set to [8 4 2 2 1], which means 8, 4, 2, 2 and 1 subsets are used in the partition for the most recent five symbols, the total number of trellis states is $8 \times 4 \times 2 \times 2 \times 1 = 128$. Thus, the complexity is reduced by $32768 \div 128 = 256$
  times compared to the MLSE.

2. The schematic for this subnetwork is shown in the following figure.
   Input data is de-rotated to eliminate phase rotation in 8PSK modulation. Next, it is split into forward and reversed-backward subframes because the training sequence is in the middle of the input frame. EDGE_ChannelEstimator is used in two paths for the two subframes to estimate the channel impulse response, then feed the estimation into the EDGE_VAProcessor which is the RSSE equalizer for EDGE receiver. Both subframes go through the EDGE_MatchedFilter to get the optimum signal to noise ratio (SNR). Then, the equalized subframes (output of EDGE_VAProcessor) are combined into one frame. Then, symbols are de-mapped to bits.



EDGE_Equalizer Schematic

References

1. ETSI Tdoc SMG2 WPB 108/98, Ericsson, EDGE Evaluation of 8-PSK.
2. G. Ungerboeck, "Adaptive maximum-likelihood receiver for carrier-modulated data-transmission system," IEEE Trans. Commun., vol. COM-22, pp. 624-636, May 1974.
3. R. D'Avella, L. Moreno, M. Sant'Agostion, "An adaptive MLSE receiver for TDMA digital mobile radio," IEEE J. Select. Areas Commun., vol. 7, pp. 122-129, Jan. 1989.
4. Pang Qinhua, Guo Yong, Li Weidong, "Synchronization design theory of demodulation for digital land mobile radio system," Journal of Beijing University of Posts and Telecommunications, vol. 18, pp. 14-21, Jun. 1995.
5. M. Vedat Eyuboglu, Shahid U. H. Qureshi, "Reduced-State Sequence Estimation with Set Partitioning and Decision Feedback," IEEE Trans. Commun., vol. 36 pp. 13-20, No. 1, January 1988.

EDGE_EqualizerAB

Description Adaptive equalizer for access bursts
Library EDGE, Equalization
Class SDFEDGE_EqualizerAB

Parameters

Name	Description	Default	Type	Range
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum	
TSC	training sequence code	0	int	[0, 2]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE	enum	
MaxDelay	maximum delay of channel in symbol duration units	5	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1	int array	†
† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$				

Pin Inputs

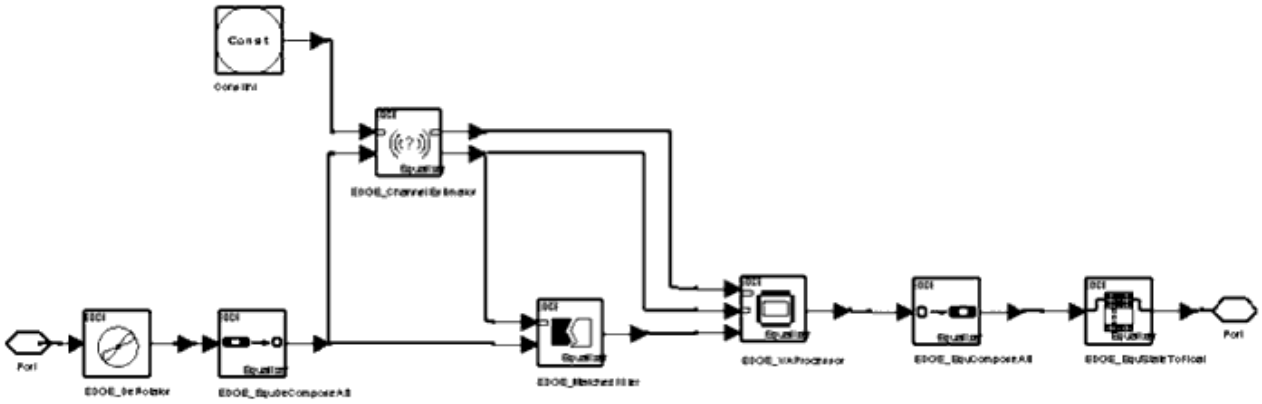
Pin	Name	Description	Signal Type
1	input	synchronized signal to be equalized	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	output	bit sequence after equalization	real

Notes/Equations

1. This subnetwork is used to restore the data sequence from the received and synchronized signals of access bursts.
   Because two new training sequences are added in EDGE Reference 6, the TSC parameter is used to indicate the training sequence.
2. The schematic for this subnetwork is shown in the following figure. Input data is split into synchronization and information sequences after being de-rotated. The synchronization sequence calculates channel estimates with which the information sequence is equalized. The synchronization and equalized information sequences are then composed.



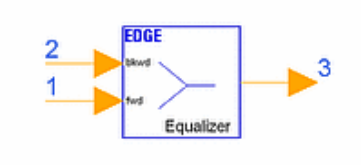
EDGE_EqualizerAB Schematic

References

1. ETSI Tdoc SMG2 WPB 108/98, Ericsson, EDGE Evaluation of 8-PSK
2. G. Ungerboeck, "Adaptive maximum-likelihood receiver for carrier-modulated data-transmission system," IEEE Trans. Commun., vol. COM-22, pp. 624-636, May 1974.
3. R. D'Avella, L. Moreno, M. Sant'Agostion, "An adaptive MLSE receiver for TDMA digital mobile radio," IEEE J. Select. Areas Commun., vol. 7, pp. 122-129, Jan. 1989.
4. Pang Qinhua, Guo Yong, Li Weidong, "Synchronization design theory of demodulation for digital land mobile radio system," Journal of Beijing University of Posts and Telecommunications, vol. 18, pp. 14-21, Jun. 1995.
5. M. Vedat Eyuboglu, Shahid U. H. Qureshi, "Reduced-State Sequence Estimation with Set Partitioning and Decision Feedback," IEEE Trans. Commun., vol. 36 pp. 13-20, No. 1, January 1998.

6. Tdoc SMG2 EDGE 2E99-403, EDGE: New training sequences for Access Burst due to EGPRS,SMG2EDGE WS #10, August 24 - 27, 1999

EDGE_EquCombiner



Description Bidirectional equalization combiner
Library EDGE, Equalization
Class SDFEDGE_EquCombiner

Parameters

Name	Description	Default	Sym	Type	Range
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK		enum	
BurstType	burst type: Normal Burst, Synchronization Burst	Normal Burst		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]

Pin Inputs

Pin	Name	Description	Signal Type
1	fwd	forward frame	int
2	bkwd	backward frame	int

Pin Outputs

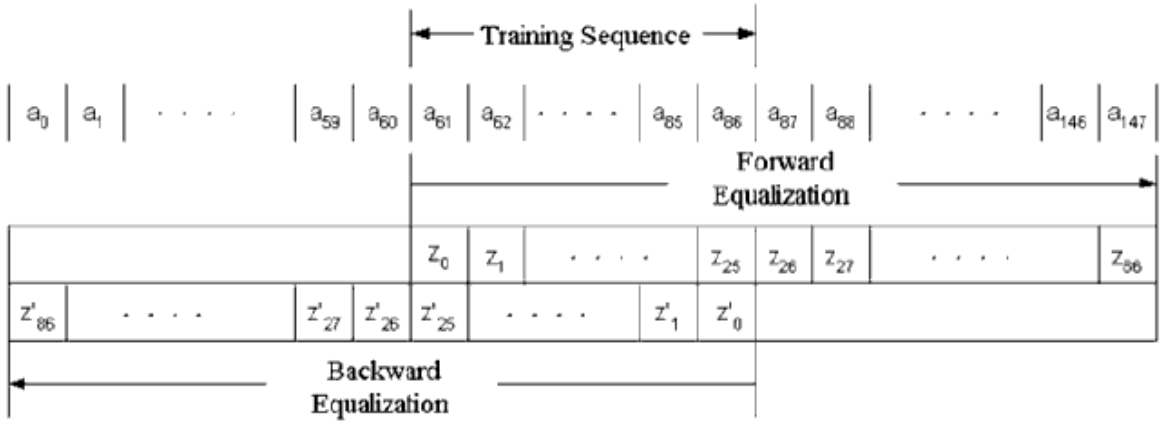
Pin	Name	Description	Signal Type
3	output	combined burst	int

Notes/Equations

1. This model is used to combine two input frames into a burst. M output tokens are produced for each N input token consumed at pins fwd and bkwd; for M and N, refer to the following table.

ModType	BurstType	M	N
GMSK	Normal Burst	156	87 + 2×L
GMSK	Synchronization Burst	156	106 + 2×L
Modified 8PSK	Normal Burst	156×3	(87 + 2×L)×3
Modified 8PSK	Synchronization Burst	156×3	(106 + 2×L)×3

2. This model combines two input frames to form a burst, as illustrated in the following figure. The forward frame starts at the beginning of the training sequence and ends at the end of the burst; the backward frame starts at the end of the training sequence and ends at the beginning of the burst in the reverse order. Since both frames contain a training sequence, only the training sequences in the forward frame is embedded in the resulting burst.
   Then eight bits of 0 (8 × 3 = 24 bits for 8PSK modulation) are added to the end as guard bits to form a normal burst. The following figure shows the split of a normal burst. The synchronization burst is implemented the same way except the length of training sequence is 64 bits for GMSK modulation (64 × 3 = 192 bits for 8PSK modulation).

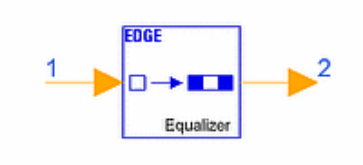


Bidirectional Equalization on Normal Burst

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 4.8.0, Nov. 1996.

EDGE_EquComposeAB



Description Equalization access burst composer
Library EDGE, Equalization
Class SDFEDGE_EquComposeAB

Parameters

Name	Description	Default	Sym	Type	Range
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]

Pin Inputs

Pin	Name	Description	Signal Type
1	input	equalized synchronizaiton and information sequence	int

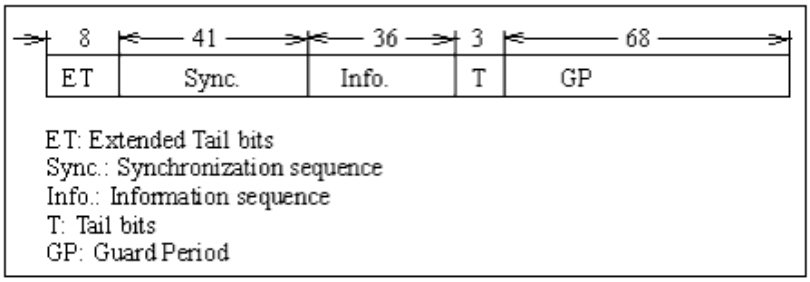
Pin Outputs

Pin	Name	Description	Signal Type
2	output	output burst	int

Notes/Equations

1. This model is used to compose the access burst in equalization. 156 output tokens are produced for each 80 + 2 × L input tokens consumed.
2. The access burst is illustrated in the following figure. There are eight extended tail bits, a synchronization sequence, an information sequence, three tail bits equal to 0, and an extended guard sequence. The extended tail bits, synchronization sequence and the extended guard sequence are defined in [1]; the information sequence is defined in [2].

This model receives the synchronization and information sequences with tail bits considering the spread of the channel and the matched filter. It composes the burst by adding extended tail bits and filling the guard period with NRZ signal 1, which is mapped to the logical signal 0.

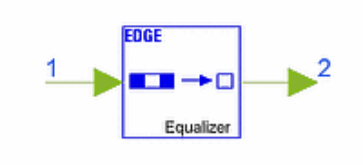


Access Burst Format

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 4.8.0, Nov. 1996.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.03, Channel Coding, version 5.1.0, May 1996.

EDGE_EquDeComposeAB



Description Equalization access burst decomposer
Library EDGE, Equalization
Class SDFEDGE_EquDeComposeAB

Parameters

Name	Description	Default	Sym	Type	Range
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]

Pin Inputs

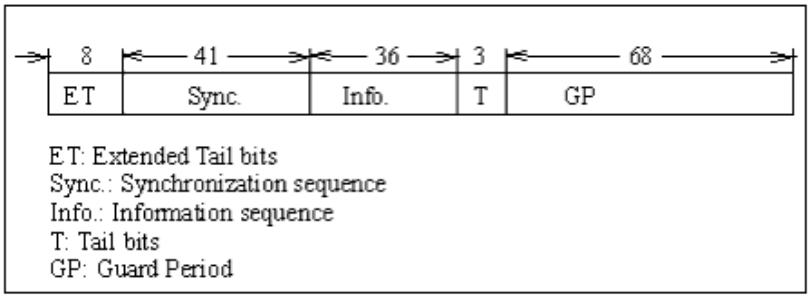
Pin	Name	Description	Signal Type
1	input	input burst	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output synchronization and information sequence	complex

Notes/Equations

1. This model is used to decompose the access burst in equalization.
   80 + 2 × L output tokens are produced for each 156 input tokens consumed.
2. The access burst is illustrated in the following figure. There are eight extended tail bits, a synchronization sequence, an information sequence, three tail bits equal to 0 and an extended guard sequence. The extended tail bits, synchronization sequence, and extended guard sequence are defined in [1]; the information sequence is defined in [2].
   This model receives the whole bit-synchronized and de-rotated burst, and outputs the synchronization and information sequences with tail bits considering the spread of the channel and the matched filter.

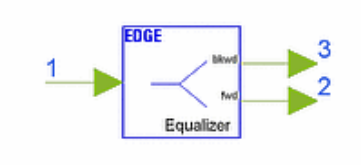


Access Burst Format

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 4.8.0, Nov. 1996.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.03, Channel Coding, version 5.1.0, May 1996.

EDGE_EquSplitter



Description Bidirectional equalization splitter
Library EDGE, Equalization
Class SDFEDGE_EquSplitter

Parameters

Name	Description	Default	Sym	Type	Range
BurstType	burst type: Normal Burst, Synchronization Burst	Normal Burst		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input burst	complex

Pin Outputs

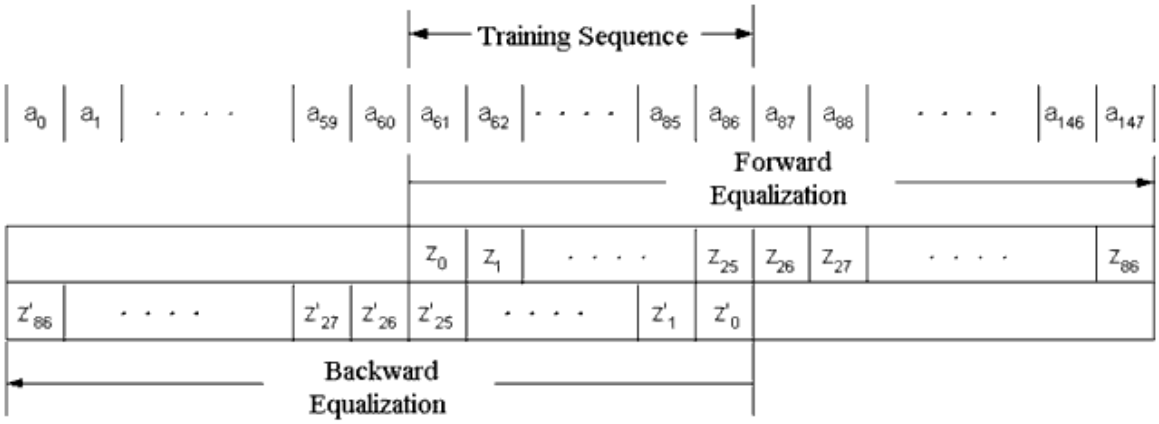
Pin	Name	Description	Signal Type
2	fwd	forward frame	complex
3	bkwd	backward frame	complex

Notes/Equations

1. This model is used to split one burst into two frames. Each firing, 156 input tokens are consumed, N output tokens at fwd and bkwd are produced, for N refer to the following table.

N	BurstType
87 + 2×L	Normal Burst
106 + 2×L	Synchronization Burst

2. This model splits one burst into two frames as illustrated in the following figure for a normal burst. The forward frame starts at the beginning of the training sequence and ends at the end of the burst; the backward frame starts at the end of the training sequence and ends at the beginning of the burst in reverse order. 0s are added to each frame to reserve space for spreading signals that will be introduced by the following matched filter. The number of 0s is determined by MaxDelay.
   By considering the spreading of signals transmitted through the channel, the backward equalization starts at the Lth bit following the end of training sequence in the implementation of this component. Implementation is the same for a synchronization burst, except the training sequence length is 64 symbols.

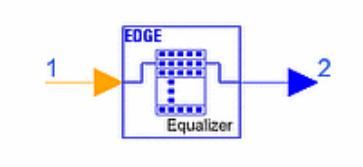


Bidirectional Equalization on Normal Burst

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 4.8.0, Nov. 1996.

EDGE_EquStateToFloat



Description State index to float translation
Library EDGE, Equalization
Class SDFEDGE_EquStateToFloat

Parameters

Name	Description	Default	Type
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum

Pin Inputs

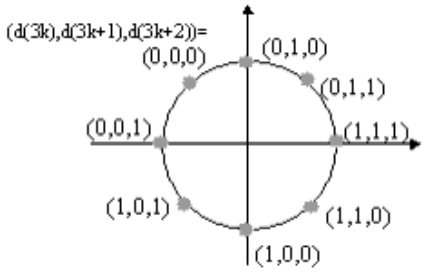
Pin	Name	Description	Signal Type
1	input	state index of equalizer signal	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	translated float numbers	real

Notes/Equations

1. This model is used to translate each input state index into one floating-point number for GMSK modulation, or three floating-point numbers for 8PSK modulation. Each floating-point number takes a value of +1 or −1. Each firing, N tokens are produced for each token consumed. When ModType is GMSK, N=1; when ModType is Modified 8PSK, N=3.
2. In 8PSK modulation, each three consecutive input bits are mapped into one 8PSK modulated symbol according to the rule of Gray-mapping illustrated in the following figure. By marking each state to an index number, the relationship between state index and input bits is obtained as listed in the following table.
   As the result of equalization, the estimated state index of each symbol is output from EDGE_VAProcessor. This model translates these indexes according to the following table, then transforms the binary bits into floating-point numbers by mapping 0 to 1 and 1 to -1.
   For GMSK modulation, only the mapping is performed because there are only two symbol states.



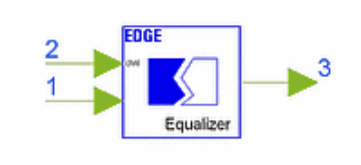
Symbol Constellation of 8PSK

State Index	Input Bits
0	0, 0, 1
1	1, 0, 1
2	1, 0, 0
3	1, 1, 0
4	1, 1, 1
5	0, 1, 1
6	0, 1, 0
7	0, 0, 0

References

1. ETSI Tdoc SMG2 WPB 108/98, Ericsson, EDGE Evaluation of 8-PSK.

EDGE_MatchedFilter



Description Matched filter
Library EDGE, Equalization
Class SDFEDGE_MatchedFilter

Parameters

Name	Description	Default	Sym	Type	Range
BurstType	burst type: Normal Burst, Synchronization Burst, Access Burst	Normal Burst		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]

Pin Inputs

Pin	Name	Description	Signal Type
1	input	derotated signal, one sample per symbol	complex
2	chnl	estimate of complex channel	complex

Pin Outputs

Pin	Name	Description	Signal Type
3	output	matched filtered data	complex

Notes/Equations

1. This model is used for matched filtering the received data. N output tokens are produced for each N token consumed at pin input and L+1 tokens are consumed at pin chnl; refer to the following table for N.

N	BurstType
87 + 2×L	Normal Burst
106 + 2×L	Synchronization Burst
80 + 2×L	Access Burst

2. This model is used for matched filtering before the Viterbi processor to establish an optimum SNR. The number of taps of the matched filter (MF) is (L+1). The MF gets its tap coefficients from EDGE_ChannelEstimator, which are the complex conjugates of the reverse sequence of the estimated CIR coefficients.
   In constructing the equalizer, the MF will be followed by a Viterbi processor, which uses a modified Viterbi algorithm [1] and operates directly on the MF output without whitening the noise.

References

1. G. Ungerboeck, "Adaptive maximum-likelihood receiver for carrier-modulated data-transmission system," IEEE Trans. Commun., vol. COM-22, pp. 624-636, May 1974.
2. R. D'Avella, L. Moreno, M. Sant'Agostion, "An adaptive MLSE receiver for TDMA digital mobile radio," IEEE J. Select. Areas Commun., vol. 7, pp. 122-129, Jan. 1989.
3. Pang Qinhua, Guo Yong, Li Weidong, "Synchronization design theory of demodulation for digital land mobile radio system," Journal of Beijing University of Posts and Telecommunications, vol. 18, pp. 14-21, Jun. 1995.

EDGE_VAProcessor

Description Viterbi algorithm processor
Library EDGE, Equalization
Class SDFEDGE_VAProcessor

Parameters

Name	Description	Default	Sym	Type	Range
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK		enum	
BurstType	burst type: Normal Burst, Synchronization Burst, Access Burst	Normal Burst		enum	
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†
† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$					

Pin Inputs

Pin	Name	Description	Signal Type
1	input	matched filtered signal, one sample per symbol	complex
2	chnl	estimate of complex channel	complex
3	index	index used to correct the synchronization	int

Pin Outputs

Pin	Name	Description	Signal Type
4	output	sequence of states of symbols after equalization	int

Notes/Equations

1. This model is used to adaptively equalize the received data. N tokens are produced at output for each N input tokens consumed at input, L+1 tokens are consumed at chnl and one token is consumed at index; refer to the following table for N.

BurstType	N
Normal Burst	87 + 2×L
Synchronization Burst	106 + 2×L
Access Burst	80 + 2×L

2. The EDGE_MatchedFilter is used before the Viterbi processor to establish an optimum SNR.
   The Viterbi processor uses a modified Viterbi algorithm [1] that operates directly on the MF output without whitening the noise. Two methods for using the modified Viterbi algorithm are integrated into the model. For GMSK modulated signals, a maximum likelihood sequence estimation (MLSE) method [1] is used; for 8PSK modulated signals in EDGE systems, the reduced-state sequence estimation (RSSE) method [4] is used to reduce the complexity of implementation.
   The index input is used with the results of the Viterbi processor to further correct the synchronization. The results are output from the offset of the value of index and 0s are added to the end.

References

1. G. Ungerboeck, "Adaptive maximum-likelihood receiver for carrier-modulated data-transmission system," IEEE Trans. Commun., vol. COM-22, pp. 624-636, May 1974.
2. R. D'Avella, L. Moreno, M. Sant'Agostion, "An adaptive MLSE receiver for TDMA digital mobile radio," IEEE J. Select. Areas Commun., vol. 7, pp. 122-129, Jan. 1989.
3. Pang Qinhua, Guo Yong, Li Weidong, "Synchronization design theory of demodulation for digital land mobile radio system," Journal of Beijing University of Posts and Telecommunications, vol. 18, pp. 14-21, Jun. 1995.
4. M. Vedat Eyuboglu, Shahid U. H. Qureshi, "Reduced-State Sequence Estimation with Set Partitioning and Decision Feedback," IEEE Trans. Commun., vol. 36 pp. 13-20, No. 1, January 1998.

Framing Components for EDGE Design Library

- *EDGE AccessBurst* (edge)
- *EDGE AddRamp* (edge)
- *EDGE DeAccessBurst* (edge)
- *EDGE DeNormalBurst* (edge)
- *EDGE DeSBurst* (edge)
- *EDGE DeTDMA* (edge)
- *EDGE DummyBurst* (edge)
- *EDGE FBurst* (edge)
- *EDGE NormalBurst* (edge)
- *EDGE SBurst* (edge)
- *EDGE TDMA* (edge)

EDGE_AccessBurst

Description Access burst construction
Library EDGE, Framing
Class SDFEDGE_AccessBurst

Parameters

Name	Description	Default	Type	Range
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum	
TSC	training sequence code	0	int	[0, 2]

Pin Inputs

Pin	Name	Description	Signal Type
1	input	encrypted bits	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	modulating bits including guarding period	int

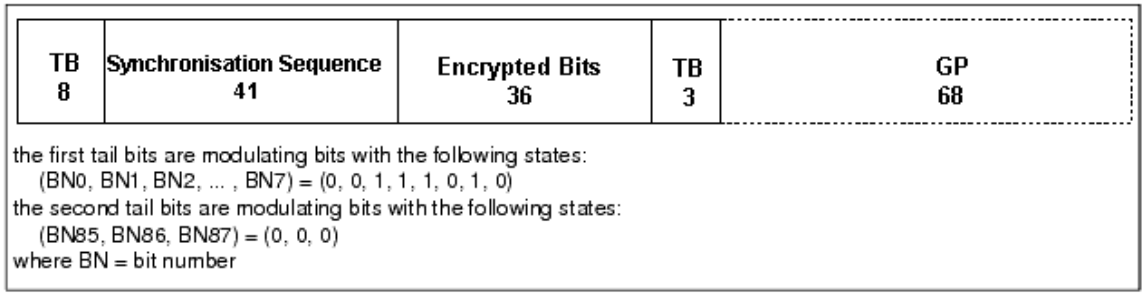
Notes/Equations

1. This model is used to construct an access burst. The number of tokens produced and consumed each firing are listed in the following table.

Tokens Consumed and Produced

ModType	Tokens Consumed	Tokens Produced
Modified 8PSK	36×3	156×3
GMSK	36	156

2. The access burst in this model, defined in GSM standard 05.02, is illustrated in the following figure. The time slot structure in EDGE systems is the same as GSM [2]. For 8PSK modulation, the number of modulated training, data and tail symbols are consistent with those in GSM systems where GMSK modulation is used. The number of modulating bits of each part in access burst for GMSK and 8PSK modulation is listed in the first of the following two tables. (Only 68 or 204 guard bits are added in this model because bit representation is not available for 0.25 or 0.75 bits.) Three training sequences are defined for access burst in EDGE and specified by TSC; the second of the following two tables lists the training sequence bits. These sequences use the BPSK subset of 8PSK symbol constellation during the midamble [2]. Therefore, training bits generated with 8PSK modulation are transformed from 41 bits to 3 × 41 = 123 bits by mapping 0 to 001 and 1 to 111.



Access Burst Format

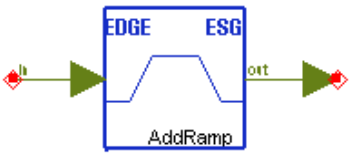
ModType	Tail Bits	Training Bits	Encrypted Bits	Guard Bits
GMSK	8+3	41	36	68.25
Modified 8PSK	(8+3)×3	123	108	204.75

TSC	Training Sequence Bits
0	0,1,0,0,1,0,1,1,0,1,1,1,1,1,1,1,0,0,1,1,0,0,1,1,0,1,0,1,0,1,0,1,0,0,0,1,1,1,1,0,0,0
1	0,1,0,1,0,1,0,0,1,1,1,1,1,0,0,0,1,0,0,0,0,0,1,1,0,0,0,1,0,1,1,1,1,0,0,1,0,0,1,1,0,1
2	1,1,1,0,1,1,1,1,0,0,1,0,0,1,1,1,0,1,0,1,0,1,1,0,0,0,0,0,0,1,1,0,1,1,0,1,1,1,0,1,1,1

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999
3. Tdoc SMG2 EDGE 2E99-403, EDGE: New Training Sequences for Access Burst due to EGPRS,SMG2EDGE WS #10, August 24 - 27, 1999

EDGE_AddRamp



Description adding ramp up and ramp down
Library EDGE, Framing
Class SDFEDGE_AddRamp

Parameters

Name	Description	Default	Type	Range
Version	EDGE specification version used for normal burst; if Version=Basic, each burst has 156 symbols else complys with GSM 8.3.0 Release 1999: Basic, GSM_8_3_0_Release_1999	Basic	enum	
TS_State	state of each time slot; 0 for idle, 1 for active	1 1 1 1 1 1 1 1	int array	[0, 1]
PwrType	power on and power off type: None, Linear, Cosine	None	enum	
RampLength	power on and power off length	4	int	[0, 156]
RampUpScramble	scramble of ramp up function	1 1 1 1	real array	(-∞, ∞)
RampDownScramble	scramble of ramp down function	1 1 1 1	real array	(-∞, ∞)
Continues	adding ramp between active slots or not: NO, YES	NO	enum	

Pin Inputs

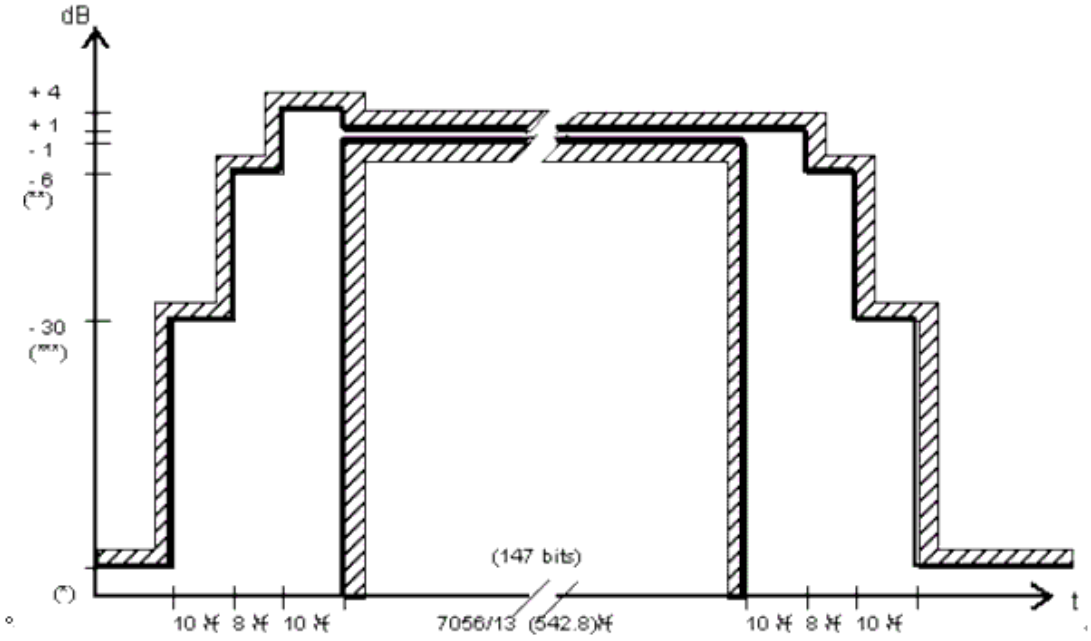
Pin	Name	Description	Signal Type
1	in	input frame	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	out	output frame	complex

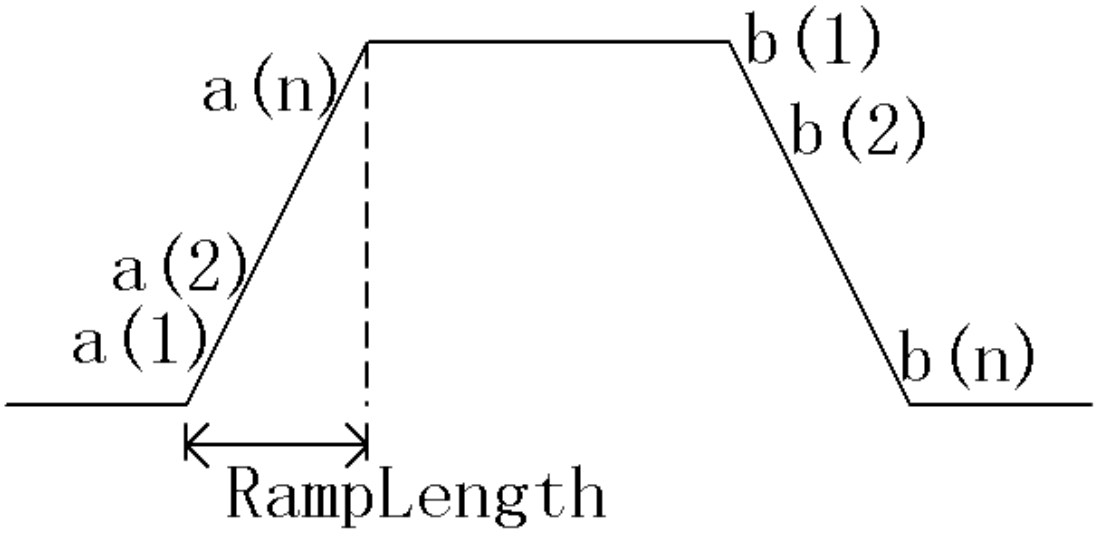
Notes/Equations:

1. This model is used to add ramp in a frame.
2. The frame shape defined in specification is as shown in the following figure. A base transceiver station is not required to have a capability to ramp down and up between adjacent bursts, but is required to have a capability to ramp down and up for non-used time-slots. If Continues is set YES, then ramp is not inserted between active slots. If Continues is set NO, then ramp is inserted between active slots. The ramp shape is defined by PwrType which has the option None, Linear and Cosine. If chosen None, no ramp will be added. The ramp length defined by Ramplength.



frame shape

3. RampUpScramble a(1), a(2),...a(n) and RampDownScramble b(1), b(2),...b(n) is used as in the following figure. They are used as float weight that can change the shape of ramp.

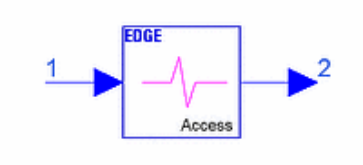


scramble

References

1. GSM 05.02, version 8.3.0, Release 1999
2. GSM 05.05, version 8.3.0, Release 1999

EDGE_DeAccessBurst



Description Access burst disassembly
Library EDGE, Framing
Class SDFEDGE_DeAccessBurst

Parameters

Name	Description	Default	Type
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	access burst bits	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encrypted bits	real

Notes/Equations

1. This model is used to disassemble an access burst. The number of tokens produced and consumed each firing are listed in the following table.

Tokens Consumed and Produced

ModType	Tokens Consumed	Tokens Produced
Modified 8PSK	156×3	36×3
GMSK	156	36

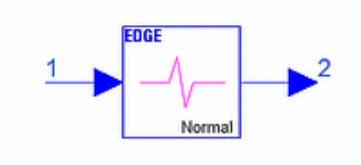
2. This model disassembles the access burst defined in GSM standard 05.02 and illustrated in the following figure. The time slot structure in EDGE systems is the same as GSM [4].
   For 8PSK modulation, the number of modulated training, data and tail symbols are consistent with those in GSM system where GMSK modulation is used; in EDGE one symbol contains three bits.

Access Burst Format

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, Addressing and Identification, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities, version 3.5.1, March 1992.
4. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17- 19, 1999
5. Tdoc SMG2 EDGE 2E99-403, EDGE: New Training Sequences for Access Burst due to EGPRS,SMG2EDGE WS #10, August 24 - 27, 1999

EDGE_DeNormalBurst



Description Normal burst disassembly
Library EDGE, Framing
Class SDFEDGE_DeNormalBurst

Parameters

Name	Description	Default	Type
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	normal burst bits	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encrypted bits	real

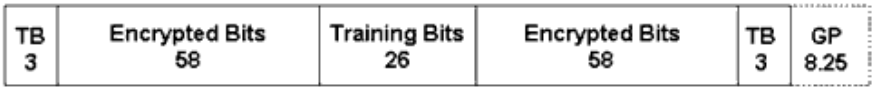
Notes/Equations

1. This model is used to disassemble a normal burst of 156 bits. The number of tokens produced and consumed each firing are listed in the following table.

Tokens Consumed and Produced

ModType	Tokens Consumed	Tokens Produced
Modified 8PSK	156×3	2×58×3
GMSK	156	2×58

2. The normal burst, defined in GSM standard 05.02, is illustrated in the following figure. The time slot structure in EDGE systems is the same as GSM [4].
For 8PSK modulation, the number of modulated training, data and tail symbols are consistent with those in GSM systems where GMSK modulation is used; in EDGE one symbol contains three bits.

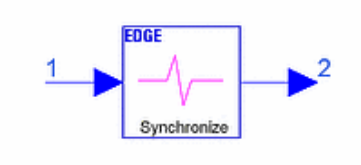


Normal Burst Format

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, Addressing and Identification, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, *Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities* , version 3.5.1, March 1992.
4. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999

EDGE_DeSBurst



Description Synchronization burst disassembly
Library EDGE, Framing
Class SDFEDGE_DeSBurst

Parameters

Name	Description	Default	Type
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	synchronization burst bits	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	encrypted bits	real

Notes/Equations

1. This model is used to disassemble a synchronization burst. The number of tokens produced and consumed each firing are listed in the following table.

Tokens Consumed and Produced

ModType	Tokens Consumed at Input	Tokens Produced at Output
Modified 8PSK	156×3	2×39×3
GMSK	156	2×39

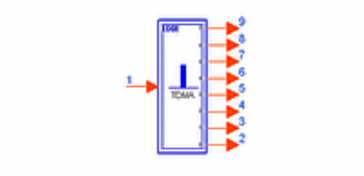
2. This model disassembles the synchronization burst defined in GSM standard 05.02 and illustrated in the following figure. The time slot structure in EDGE systems is the same as GSM [4].
   For 8PSK modulation, the number of modulated training, data and tail symbols are consistent with those in GSM systems where GMSK modulation is used.

Synchronization Burst Format

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, Addressing and Identification, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, *Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities* , version 3.5.1, March 1992.
4. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999.

EDGE_DeTDMA



Description TDMA frame disassembly
Library EDGE, Framing
Class SDFEDGE_DeTDMA

Parameters

Name	Description	Default	Type	Range
BitsPerSlot	number of bits per time slot	468	int	[1, ∞) See Note 3

Pin Inputs

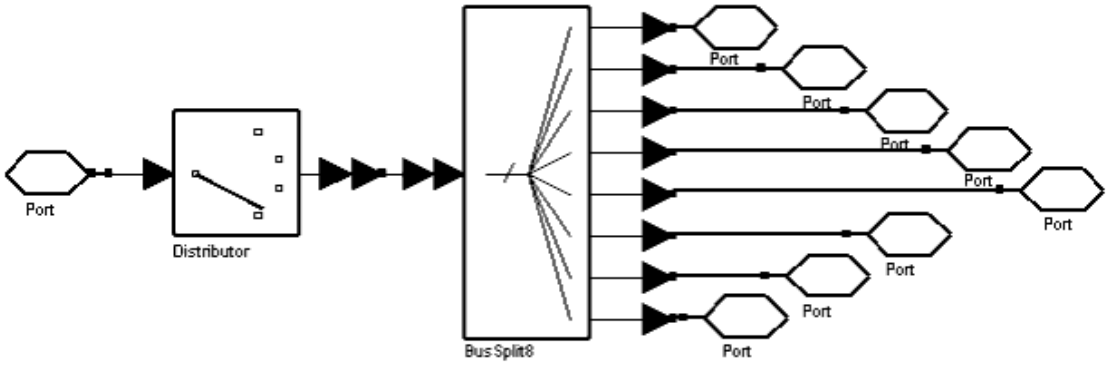
Pin	Name	Description	Signal Type
1	input	one TDMA frame consists of eight time slots	anytype

Pin Outputs

Pin	Name	Description	Signal Type
2	TN0	data for time slot 0	anytype
3	TN1	data for time slot 1	anytype
4	TN2	data for time slot 2	anytype
5	TN3	data for time slot 3	anytype
6	TN4	data for time slot 4	anytype
7	TN5	data for time slot 5	anytype
8	TN6	data for time slot 6	anytype
9	TN7	data for time slot 7	anytype

Notes/Equations

1. This subnetwork is used to disassemble one TDMA frame into eight time slots.
2. The schematic for this subnetwork is shown in the following figure. It consists of BusSplit and Distributor models.



EDGE_DeTDMA Schematic

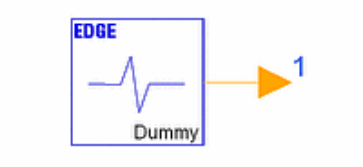
3. According to the GSM standard, one TDMA frame contains eight time slots, TN0 through TN7. The designer must select a time slot in which to fill the input data. For example, if TN2 and TN4 are selected, the first input bits or symbols of the subnetwork will be placed into TN2 and the second will be placed into TN4; the idle time slots will be filled with 0.
   The number of bits consumed in each time slot is defined by BitsPerSlot.
   - To disassemble a frame with all eight time slots modulated by GMSK, set BitsPerSlot to 156; when modulated by 8PSK, set BitsPerSlot to 468.
   - To disassemble a mixed frame (for example, some of the eight time slots are to be GMSK modulated, others are to be 8PSK modulated) set BitsPerSlot to 468. In this case, each bit of the output GMSK demodulating bursts should be repeated three times using Repeat components before EDGE_DeTDMA in order for all eight input time slots to have the same length. After EDGE_DeTDMA, the

bit repeated GMSK bursts are recovered using DownSample components.

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, Addressing and Identification, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, *Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities* , version 3.5.1, March 1992.

EDGE_DummyBurst



Description Dummy burst construction
Library EDGE, Framing
Class SDFEDGE_DummyBurst

Parameters

Name	Description	Default	Type
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum

Pin Outputs

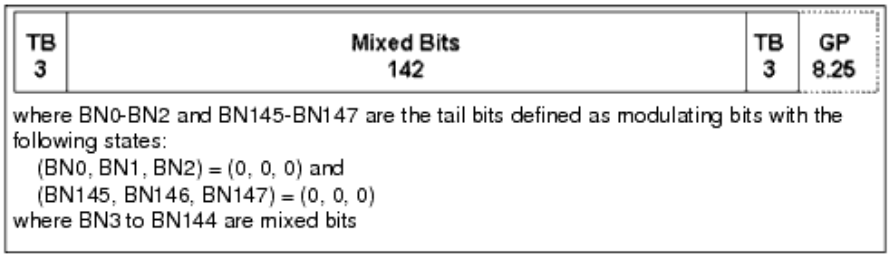
Pin	Name	Description	Signal Type
1	output	modulating bits or symbols including guarding period	int

Notes/Equations

1. This model is used to construct a dummy burst. The number of tokens produced each firing is listed in the following table.

ModType	Tokens Produced
Modified 8PSK	156×3
GMSK	156

2. The dummy burst, defined in GSM 05.02, is illustrated in the following figure. The time slot structure in EDGE systems is the same as GSM [4].



Dummy Burst Format

For 8PSK modulation, the number of mixed and tail symbols are consistent with those in GSM systems where GMSK modulation is used. The number of modulating bits of each part in a dummy burst for GMSK and 8PSK modulation is listed in the following table. In EDGE, dummy burst bits for 8PSK modulation are transformed from 148 to 3×148=444 bits by mapping 0 to 001 and 1 to 111.

ModType	Tail Bits	Mixed Bits	Guard Bits
Modified 8PSK	2×3×3	142×3	24.75
GMSK	2×3	142	8.25

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, Addressing and Identification, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, *Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities* , version 3.5.1, March 1992.
4. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999.

EDGE_FBurst

Description Frequency correction burst construction
Library EDGE, Framing
Class SDFEDGE_FBurst

Parameters

Name	Description	Default	Type
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum

Pin Outputs

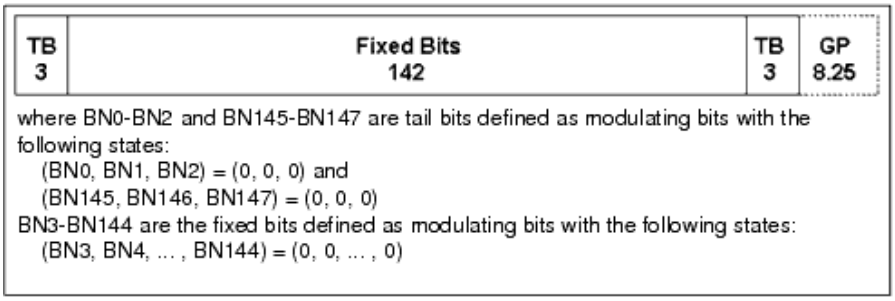
Pin	Name	Description	Signal Type
1	output	modulating bits or symbols including guarding period	int

Notes/Equations

1. This model is used to construct a frequency correction burst. The number of tokens produced each firing is listed in the following table.

ModType	Tokens Produced
Modified 8PSK	156×3
GMSK	156

2. The frequency correction burst, defined in GSM 05.02, is illustrated in the following figure. The time slot structure in EDGE systems is the same as GSM [4]. For 8PSK modulation, the number of fixed and tail symbols are consistent with those in GSM systems where GMSK modulation is used.
   In the TDMA frame construction, the frequency correction burst must be assigned to time slot 0. The number of modulating bits of each part in a frequency correction burst for GMSK and 8PSK modulation is listed in the following table. In EDGE, when generating frequency correction burst bits for 8PSK modulation, it is transformed from 148 bits to 3 × 148 = 444 bits by mapping 0 to 001 and 1 to 111.



Frequency Correction Burst Format

ModType	Tail Bits	Fixed Bits	Guard Bits
Modified 8PSK	2×3×3	142×3	24.75
GMSK	2×3	142	8.25

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, Addressing and Identification, version 3.5.1, March 1992.

3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, *Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities* , version 3.5.1, March 1992.
4. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999

EDGE_NormalBurst

Description Normal burst construction for EDGE
Library EDGE, Framing
Class SDFEDGE_NormalBurst

Parameters

Name	Description	Default	Type	Range
Version	EDGE specification version used for normal burst; if Version=Basic, each burst has 156 symbols else complys with GSM 8.3.0 Release 1999: Basic, GSM_8_3_0_Release_1999	Basic	enum	
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum	
TSC	training sequence code, if Version=GSM 8.3.0 Release 1999, TSC will be ignored with default TSC0	0	int	[0, 7]
ExtraSymbol	add extra symbol to normal burst, if Version=Basic, ExtraSymbol will be ignored with default no: yes, no	no	enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	input	information bits	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	modulating bits with guarding period	int

Notes/Equations

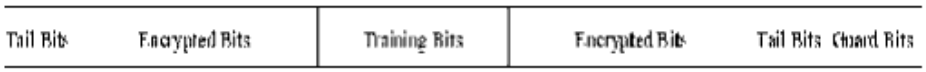
1. This model is used to construct a basic or ESG-compatible normal burst with the format defined in GSM 05.02 standard version 8.3.0 Release 1999.
   The number of tokens produced and consumed each firing is listed in the following table.

ModType	Tokens Consumed	Tokens Produced	
Modified 8PSK	2×58×3	156×3	157×3 (1 extra symbol for guard)
GMSK	2×58	156	157 (1 extra symbol for guard)

2. The GSM normal burst format is illustrated in the following figure. The time slot structure in EDGE systems is the same as GSM [4].
   For 8PSK modulation, the number of modulated training, data and tail symbols are consistent with those in GSM systems where GMSK modulation is used. The following figure lists the number of modulating bits of each part in a normal burst for GMSK and 8PSK modulation.
   ExtraSymbol will determine if an extra symbol needs to be added to this burst to implement 0.25- or 0.75-bits for a TDMA frame. Thus the number of guard bits in this model will be 8 or 9 for GMSK and 24 or 27 for 8PSK.
   The payload per burst becomes 348 bits for 8PSK modulation and 116 bits for GMSK modulation. Stealing bits are included in the encrypted bits.
   There are 8 different training sequences defined by GSM for Basic normal burst and specified by TSC (training sequence code). For GMSK modulation, the following table lists the training sequence bits according to TSC.

ModType	Tail Bits	Training Bits	Encrypted Bits	Guard Bits
Modified 8PSK	2×9	78	2×(171+3)	24.75
GMSK	2×3	26	2×(57+1)	8.25

   For 8PSK modulation compatibility with ESG (GSM 8.3.0 Release 1999) another 8 TSC formats are used. The following table lists the training sequence (hexadecimal) formats according to TSC.
   For *GSM 8.3.0 Release 1999* , the TSC for 8PSK is derived by mapping 1 bit of TSC for GMSK to 3 bits 001 of 8PSK and accordingly 0 bit to 111. For *Basic* the TSC for 8PSK is derived by mapping 1 bit of TSC for GMSK to 3 bits 111, and 0 bit to 001.



Normal Burst Format

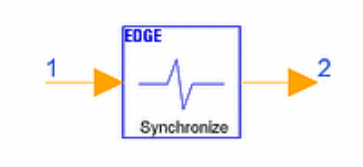
TSC	Training Sequence Bits
0	0,0,1,0,0,1,0,1,1,1,0,0,0,0,1,0,0,0,1,0,0,1,0,1,1,1
1	0,0,1,0,1,1,0,1,1,1,0,1,1,1,1,0,0,0,1,0,1,1,0,1,1,1
2	0,1,0,0,0,0,1,1,1,0,1,1,1,0,1,0,0,1,0,0,0,0,0,1,1,1,0
3	0,1,0,0,0,1,1,1,1,0,1,1,0,1,0,0,0,1,0,0,0,1,1,1,1,0
4	0,0,0,1,1,0,1,0,1,1,1,0,0,1,0,0,0,0,0,1,1,0,1,0,1,1
5	0,1,0,0,1,1,1,0,1,0,1,1,0,0,0,0,0,0,1,0,0,1,1,1,0,1,0
6	1,0,1,0,0,1,1,1,1,1,0,1,1,0,0,0,1,0,1,0,0,1,1,1,1,1
7	1,1,1,0,1,1,1,1,0,0,0,1,0,0,1,0,1,1,1,0,1,1,1,1,0,0

TSC	Training Sequence Formats
0	3,F,3,F,9,E,4,9,F,F,F,3,F,F,3,F,9,E,4,9
1	3,F,3,C,9,E,4,9,E,4,9,3,F,F,3,C,9,E,4,9
2	3,9,F,F,F,2,4,F,2,4,F,3,F,9,F,F,F,2,4,F
3	3,9,F,F,9,2,4,F,2,7,9,F,F,9,F,F,9,2,4,F
4	3,F,E,4,F,3,C,9,3,F,9,F,F,F,E,4,F,3,C,9
5	3,9,F,C,9,3,C,F,2,7,F,F,F,9,F,C,9,3,C,F
6	0,F,3,F,9,2,4,9,E,4,F,F,C,F,3,F,9,2,4,9
7	0,9,3,C,9,2,7,F,E,7,F,3,C,9,3,C,9,2,7,F

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, Addressing and Identification, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, *Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities* , version 3.5.1, March 1992.
4. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999.

EDGE_SBurst



Description Synchronization burst construction
Library EDGE, Framing
Class SDFEDGE_SBurst

Parameters

Name	Description	Default	Type
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum

Pin Inputs

Pin	Name	Description	Signal Type
1	input	encrypted bits	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	modulating bits including guarding period	int

Notes/Equations

1. This model is used to construct a synchronization burst. The number of tokens produced and consumed for each firing are listed in the following table.

ModType	Tokens Consumed	Tokens Produced
Modified 8PSK	2×39×3	156×3
GMSK	2×39	156

2. The synchronization burst, defined in GSM standard 05.02, is illustrated in the following figure. The time slot structure in EDGE systems is the same as GSM [4]. For 8PSK modulation, the number of modulated training, data and tail symbols are consistent with those in GSM system where GMSK modulation is used.
The extended training bits is defined as:

   (BN42,BN43, ... ,BN105) =

   (1, 0, 1, 1, 1, 0, 0, 1, 0, 1, 1, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1, 0, 0, 1, 0, 1, 1, 0, 1, 0, 1, 0, 0, 0, 1, 0, 1, 0, 1, 1, 1, 0, 1, 1, 0, 0, 0, 0, 1, 1, 0, 1, 1)

   The same training sequence is used in EDGE by using the BPSK subset of the 8PSK symbols constellation during the midamble [4]. Therefore, training bits generated for 8PSK modulation are transformed from 64 bits to 3 × 64 = 192 bits by mapping 0 to 001 and 1 to 111.

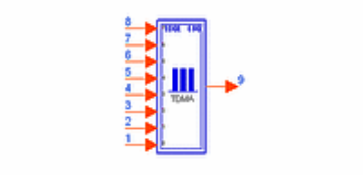
Synchronization Burst Structure

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, Addressing and Identification, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, *Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities* , version 3.5.1, March 1992.

4. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999.

EDGE_TDMA



Description TDMA frame constructor
Library EDGE, Framing
Class SDFEDGE_TDMA

Parameters

Name	Description	Default	Type	Range
Version	EDGE specification for normal burst; if choose Basic, each burst has 156 symbols, otherwise complys with GSM 8.3.0 Release 1999: Basic, GSM_8_3_0_Release_1999	Basic	enum	
BitsPerSlot	number of bits per slot; disabled if Version=GSM 8.3.0 Release 1999	468	int	[1, ∞) See Note 2

Pin Inputs

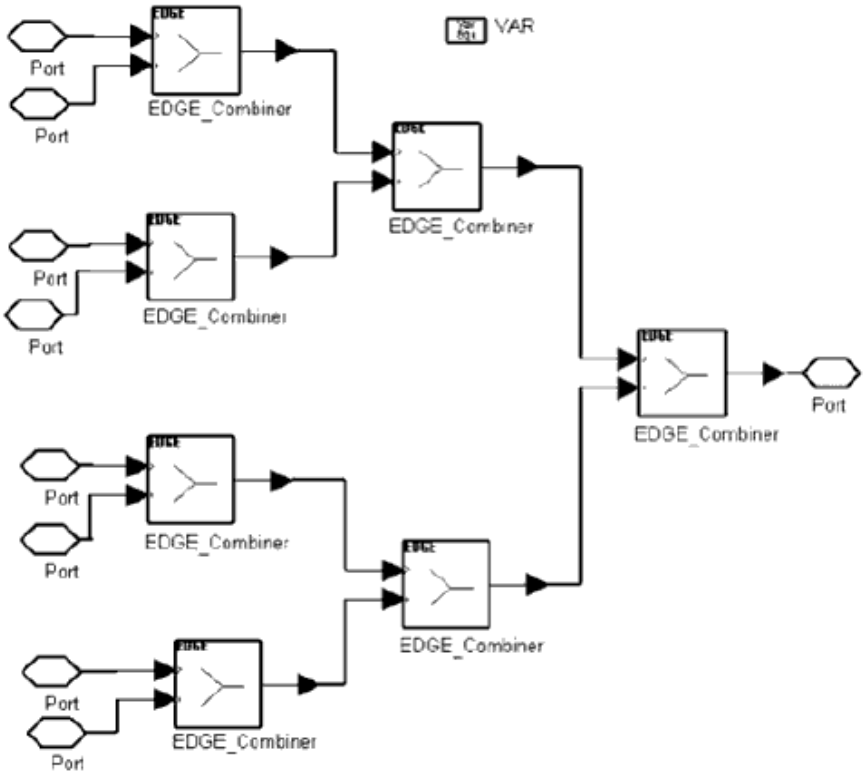
Pin	Name	Description	Signal Type
1	TN0	data for time slot 0	anytype
2	TN1	data for time slot 1	anytype
3	TN2	data for time slot 2	anytype
4	TN3	data for time slot 3	anytype
5	TN4	data for time slot 4	anytype
6	TN5	data for time slot 5	anytype
7	TN6	data for time slot 6	anytype
8	TN7	data for time slot 7	anytype

Pin Outputs

Pin	Name	Description	Signal Type
9	output	combination of TN0 to TN7 to form a EDGE TDMA frame	anytype

Notes/Equations

1. This subnetwork is used to construct one TDMA frame. The schematic for this subnetwork is shown in the following figure.

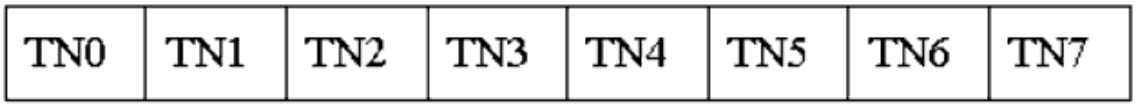


EDGE_TDMA Schematic

2. In GSM standard, one TDMA frame contains eight time slots TN0 to TN7. Each designer must select a time slot to fill the input data into it.

- When BurstSpecVersion= *Basic* , the number of bits consumed each firing at each input port is defined by BitsPerSlot.
  - To construct a frame with all eight time slots to be GMSK modulated, set BitsPerSlot to 156.
  - To construct a frame to be 8PSK modulated set BitsPerSlot to 468.
  - To form a mixed frame (some time slots are to be GMSK modulated, some are to be 8PSK modulated) set BitsPerSlot to 468. In this case, each bit of the input GMSK modulating bursts should be repeated three times by using Repeat components before EDGE_TDMA to keep all eight input time slots having the same length. Before GMSK modulation, the bit repeated GMSK bursts should be recovered by using DownSample components.
- When BurstSpecVersion= *GSM_8_3_0_Release_1999* , each firing 471 bits are consumed at TN0 and at TN4 and 468 bits at each of the other input ports.

- Data from the 8 input ports are then combined in sequence from TN0 to TN7 to form one TDMA frame as shown in the following figure.



TDMA Frame Structure

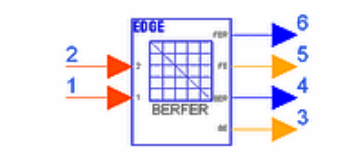
References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, Addressing and Identification, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, *Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities* , version 3.5.1, March 1992.
4. GSM 05.02, version 8.3.0, Release 1999.

Measurement Components for EDGE Design Library

- *EDGE BERFER* (edge)
- *EDGE EVM* (edge)
- *EDGE EVM Meas* (edge)
- *EDGE EVM WithRef* (edge)
- *EDGE FreqErr OffsetSupp Meas* (edge)
- *EDGE FrequencyErr* (edge)
- *EDGE NonLinearAmp* (edge)
- *EDGE Pwr Meas* (edge)
- *EDGE Pwr vs Time Meas* (edge)
- *EDGE RCWindow RCFilter* (edge)
- *EDGE SigPowerMeasure* (edge)
- *EDGE TxORFS Modulation Meas* (edge)
- *EDGE TxORFS Switching Meas* (edge)

EDGE_BERFER



Description BER and FER performance
Library EDGE, Measurement
Class SDFEDGE_BERFER

Parameters

Name	Description	Default	Sym	Type	Range
Start	frame from which measurement starts	DefaultNumericStart	F1	int	[0, ∞)
Stop	frame at which measurement stops; -1 for no stop	DefaultNumericStop	F2	int	[F1, ∞)†
FrameLength	number of bits in a frame	1	N	int	[1, ∞)
† when set to -1, measurement starts from the F1th frame and stops only when simulation stops.					

Pin Inputs

Pin	Name	Description	Signal Type
1	in1	input of the expected sequence or estimated sequence	anytype
2	in2	input of the expected sequence or estimated sequence	anytype

Pin Outputs

Pin	Name	Description	Signal Type
3	BE	sum of bit errors from the beginning of simulation	int
4	BER	output BER	real
5	FE	sum of frame error from the begining of simulation	int
6	FER	output FER	real

Notes/Equations

This model is used to calculate the system bit error rate (BER) and frame error rate (FER). The Monte Carlo method is used to calculate from the F1th to the F2th frame.

One output token is produced for each N tokens consumed.

Data sequences at in1 and in2 must be synchronized before they are imported.

EDGE_EVM

Description Single-path EVM measurement for EDGE
Library EDGE, Measurement
Class SDFEDGE_EVM

Parameters

Name	Description	Default	Sym	Unit	Type	Range
StartSym	start symbol	142			int	[0, ∞)
SymBurstLen	number of symbols within burst to be measured	142			int	[1, 10000]
SampPerSym	number of samples per symbol	16	S		int	[1, ∞)
NumBursts	number of bursts to be measured	5			int	[1, ∞)†
MeasType	type of measurement: EVM_rms, EVM_peak, EVM_95th_percentile	EVM_rms			enum	
SymbolRate	symbol rate	(1625/6) kHz		Hz	real	(0, ∞)††
EVMValue	EVM value expression options: EVM_Ratio, EVM_Percent	EVM_Ratio			enum	

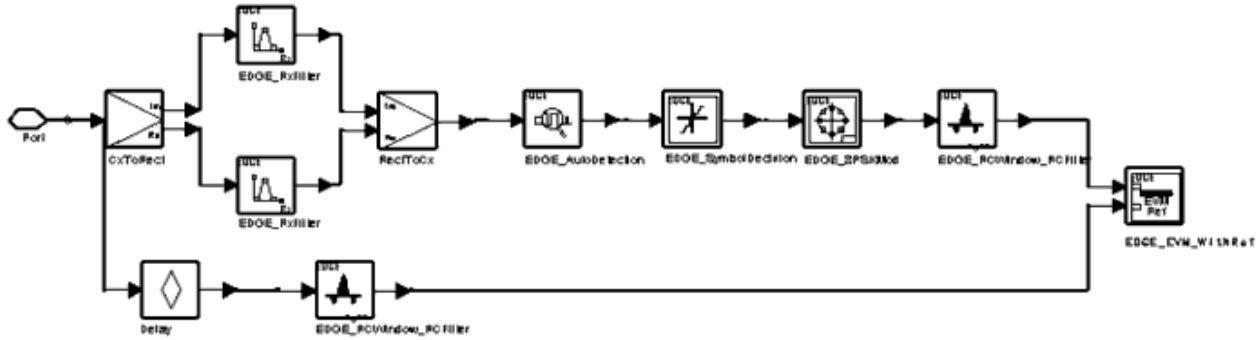
† EVM results are determined by the number of bursts indicated by NumBursts, which indicates the number of bursts to be measured and averaged.†† The simulation symbol rate is used to calculate frequency offset; the default value of 270.833 kHz is the symbol rate of EDGE/GSM.

Pin Inputs

Pin	Name	Description	Signal Type
1	input	signals to be measured for EVM	complex

Notes/Equations

1. This subnetwork is the single-path/input EVM model for EDGE. It is implemented by adding automatic EDGE reference signal generation to the two-path EVM model EDGE_EVM_WithRef.
2. The schematic for this subnetwork is shown in the following figure.
   The upper path of the two paths is the reference path. Received signals are demodulated by being passed through EDGE_RxFilter (which acts as the equalizer), EDGE_AutoDetection and EDGE_SymbolDecision. The original transmitted bits are retrieved and re-modulated to act as the reference signals.
   EDGE_RCWindow_RCFilter is used in both paths.
   To automatically detect the optimal down-sampling phase and accomplish de-rotation, EDGE_AutoDetection introduces a symbol delay of 499 in the reference path. Other delays are introduced by EDGE_RxFilter and re-modulation. So the StartSym of the EDGE_EVM_WithRef is set to 599 to input data after the delayed symbols. The delay in test path is set to be 509 = 499 + 10 symbols because the total delay of the modulation and RxFilter is a 10-symbol interval. At the EDGE_EVM_WithRef input, signals in the test path are 0- to (S−1)-sample delayed compared to those in the reference path. SymDelayBound of EDGE_EVM_WithRef is set to 2 to automatically compensate for this delay.



EDGE_EVM Schematic

EDGE_EVM_Meas

Description ESG/VSA Compatible EVM measurement
Library EDGE, Measurement
Class TSDFEDGE_EVM_Meas

Parameters

Name	Description	Default	Unit	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
MeasType	type of measurement: EVM_rms, EVM_peak, EVM_95th_percentile	EVM_rms		enum	
TS_Measured	time slot to be measured in each TDMA frame,0 to 7.	0		int	[0, 7]
TS_Num	number of time slots measured	5		int	[1, ∞)†
RIn	input resistance	50.0 Ohm	Ohm	real	[0, ∞)
RTemp	temperature of resistor in degrees Celsius; value cannot be swept	-273.15		real	[-273.15, ∞)
EVMValue	EVM value expression options: EVM_Ratio, EVM_Percent	EVM_Ratio		enum	

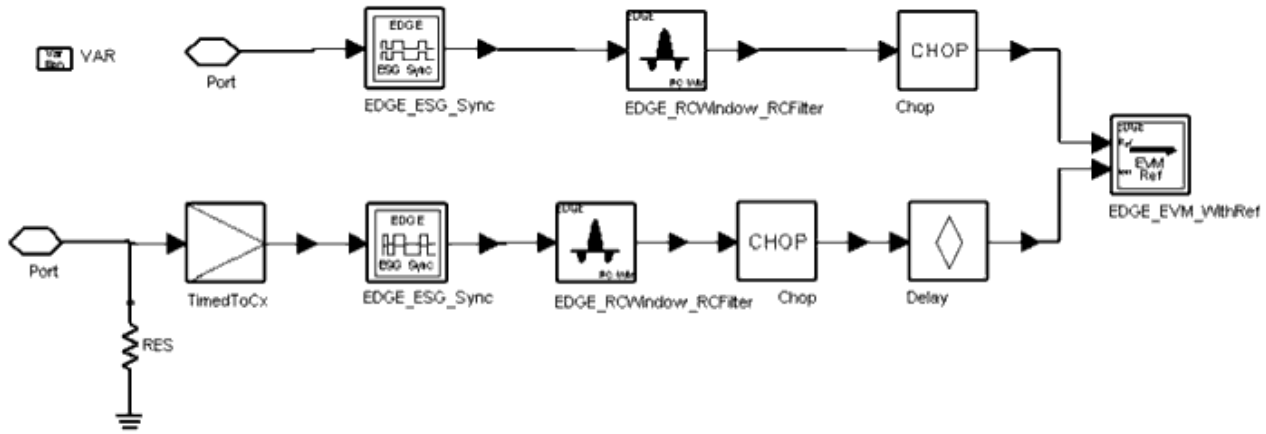
† EVM results are determined over multiple bursts; TS_Num indicates the number of bursts to be measured and averaged.

Pin Inputs

Pin	Name	Description	Signal Type
1	data	signals to be measured for EVM	timed
2	ref	reference signals for EVM measurement	complex

Notes/Equations

1. This subnetwork is used to perform error vector magnitude (EVM) measurements. This subnetwork is in compliance with EVM measurement specifications described in GSM 11.10, version 8.1.0, release 1999, and Option 202 of the Agilent E4406A VSA. One symbol is consumed each firing.
2. The schematic for this measurement subnetwork is shown in the following figure; it includes synchronization, measurement filtering, and the EVM measurement subnetwork.



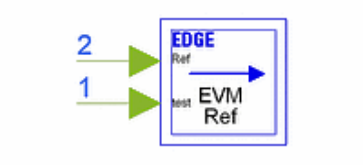
EDGE_EVM_Meas Schematic

Reference data for the EVM measurement passes through the upper path and is input to the core EVM calculation EDGE_EVM_WithRef subnetwork; test data passes through the lower path to the core EVM calculation EDGE_EVM_WithRef subnetwork. The EDGE_ESG_Sync subnetwork performs synchronization in both paths. It determines the delay in the data flow by correlating the training sequences in the data flow and those generated locally; it prefixes the data flow with 0s so the real starting point of the data flow is located at the start symbol of the second framing. That is, the first framing is filled with 0s and useless samples (which are before the sampling point of the first symbol) for the sake of synchronization.
EDGE_RCWindow_RCFilter is a raised-cosine windowed raised-cosine filter defined as the EDGE EVM measurement filter.
The Chop component is used to select the burst that will be tested from a frame. It also selects the useful-part symbols in that burst; all other symbols are discarded. The burst (time slot) to be measured is specified by the TS_Measured parameter.
The Delay component inserts a 1-symbol delay in the test data path to ensure the test path is delayed for the measurement. EDGE_EVM_WithRef performs the core calculations of the measurement. For details and formulas for calculation regarding EVM measurements refer to EDGE_EVM_WithRef documentation.

References

1. Tdoc SMG7 022/00 version 420, CR 11.10, Introduction of EGPRS Transmitter Tests for Frequency Error, Power, ORFS and Intermodulation Attenuation, 13.17.1, March 22-24, 2000.
2. ETSI SMG2 EDGE Tdoc 370r1/99, Modulation accuracy for EDGE MS and BTS, August 24-27, Paris, France, 1999.
3. GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 8.3.0, Release 1999.
4. GSM 05.10, Radio subsystem synchronization, version 3.5.1, October 1992.

EDGE_EVM_WithRef



Description EVM measurement with reference signal input
Library EDGE, Measurement
Class SDFEDGE_EVM_WithRef

Parameters

Name	Description	Default	Unit	Type	Range
StartSym	start symbol	142		int	[0, ∞)
SymBurstLen	number of symbols within burst to be measured	142		int	[1, 10000]
SampPerSym	number of samples per symbol	16		int	[1, 256]
SymDelayBound	upper bound of delay detection, in symbol, -1 for no detection	3		int	[-1, ∞)†
NumBursts	number of bursts to be measured	5		int	[1, ∞)††
MeasType	type of measurement: EVM_rms, EVM_peak, EVM_95th_percentile	EVM_rms		enum	
SymbolRate	symbol rate	(1625/6) kHz	Hz	real	(0, ∞)†††
EVMValue	EVM value expression options: EVM_Ratio, EVM_Percent	EVM_Ratio		enum	

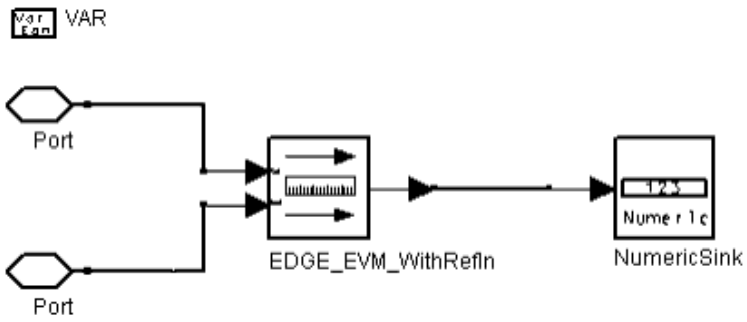
† The model fulfills the synchronization (detects the delay of test signals, and aligns them with the reference signals) inside this boundary. If set to -1, synchronization will not be applied.†† EVM results are determined over multiple bursts; NumBursts indicates the number of bursts to be measured and averaged. ††† SymbolRate is used to calculate the frequency offset; the default value 270.833 kHz is the symbol rate of EDGE/GSM.

Pin Inputs

Pin	Name	Description	Signal Type
1	testDataInput	signals to be measured for EVM	complex
2	RefDataInput	reference signals for EVM measurement	complex

Notes/Equations

1. This subnetwork is used to accomplish the EVM measurement with numeric signals in baseband. This subnetwork wraps up the EVM measurement model EDGE_EVM_WithRefIn and a numeric sink (see the following figure) to function as a typical EVM sink.



EDGE_EVM_WithRef Schematic

2. EVM measurements are used to evaluate the modulation accuracy of modulators. For example, in the IS-54 TDMA digital cellular, they are used to set the minimum specifications for the accuracy of p /4-DQPSK modulators.
The defining equations are derived from those defined in GSM 05.05 with some modifications for EDGE.
Typically, the measurement is calculated at the symbol times within one burst. Z(k) is the complex vector produced by observing the real transmitter at the optimal phase of symbol k. S(k) is the reference (ideal) signal of symbol k sampled at the same phase as that of Z(k). The transmitter model is

$$Z(k) = \{C0 + C1 \times [S(k) + E(k)]\} \times W^k$$

where

W = $e^{dr + jda}$ accounts for both a frequency offset giving *da* radians per symbol phase rotation and an amplitude change of *dr* nepers per symbol

C0 is a constant origin offset representing quadrature modulator imbalance

C1 is a complex constant representing the arbitrary phase and output power of the transmitter

E(k) is the residual vector error on sample S(k), and the value range of k is K which is [0,L-1]. By setting the parameter StartSym, designers can select which symbol the simulation starts with (S^{th} symbol). By setting the parameter SymBurstLen, designers can select the length of the burst to be

measured (L).

The error vector E(k) is measured and calculated for each instance k.

$$E(k) = \left[\frac{Z(k) \times W^{-k} - C0}{C1}\right] - S(k)$$

The sum square vector error for each component is calculated over one burst. The relative RMS vector error is defined as

$$\text{RMS EVM} = \sqrt{\frac{\sum_{k \in K} |E(k)|^2}{\sum_{k \in K} |S(k)|^2}}$$

The symbol EVM at symbol k is defined as

$$EVM(k) = \sqrt{\frac{|E(k)|^2}{\frac{\sum_{k \in K} |S(k)|^2}{K}}}$$

which is the vector error length relative to the root average energy of the burst.
C0, C1 and W are used to minimize RMS EVM per burst, then calculate the individual vector errors E(k) on each symbol. The symbol timing phase of the receiver output samples to calculate the vector error give the lowest value for RMS EVM; this phase is called the optimal phase.

- RMS EVM (MeasType=EVM_rms) for one burst is defined as

  $$\text{RMS EVM} = \sqrt{\frac{\sum_{k \in K} |E(k)|^2}{\sum_{k \in K} |S(k)|^2}}$$

  The RMS EVM should be measured by averaging over multiple bursts.
- Peak EVM (MeasType=EVM_peak) is the peak error deviation within a burst, that is, the maximum of E(k), measured at each symbol interval.
  Peak EVM should be measured by averaging over multiple bursts.
- 95th percentile (MeasType=EVM_95th_percentile) is the point where 95% of the individual EVM (EVM(k)), measured at each symbol interval, is below that point. That is, only 5% of the symbols are allowed to have an EVM exceeding the 95th-percentile point.
  The 95th percentile should be measured by averaging over multiple bursts.

References

1. ETSI SMG2 EDGE Tdoc 370r1/99, Modulation accuracy for EDGE MS and BTS, August 24-27, Paris, France, 1999

EDGE_FreqErr_OffsetSupp_Meas

Description ESG/VSA Compatible frequency error and origin offset suppression measurement
Library EDGE, Measurement
Class TSDFEDGE_FreqErr_OffsetSupp_Meas

Parameters

Name	Description	Default	Unit	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
MeasType	type of measurement: frequency error, origin offset suppression	frequency error		enum	
TS_Measured	time slot to be measured in each TDMA frame,0 to 7.	0		int	[0, 7]
TS_Num	number of time slots measured	5		int	[1, ∞)
RIn	input resistance	50.0 Ohm	Ohm	real	[0, ∞)
RTemp	temperature of resistor in degrees Celsius; value cannot be swept	-273.15		real	[-273.15, ∞)

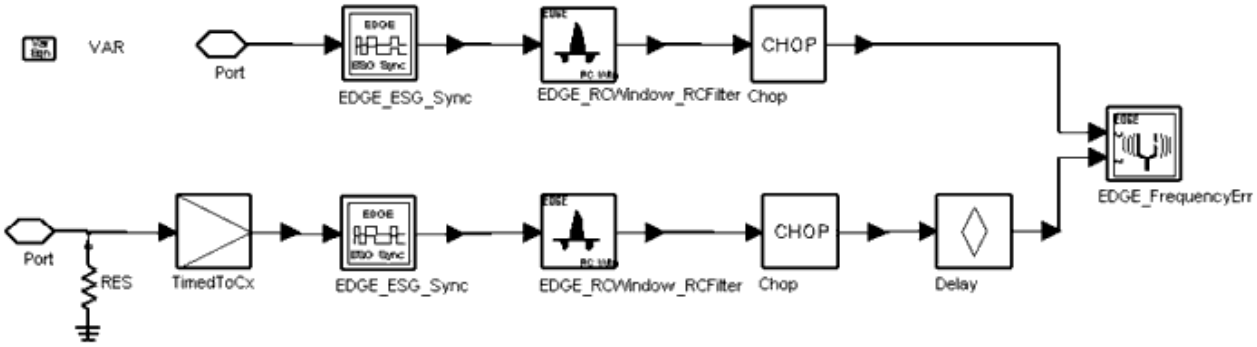
Pin Inputs

Pin	Name	Description	Signal Type
1	data	signals to be measured	timed
2	ref	reference signals	complex

Notes/Equations

This subnetwork is used to measure frequency error and origin offset suppression (OOS). One symbol is consumed each firing. The schematic for this measurement subnetwork is shown in the following figure; it includes synchronization, measurement filtering, and the frequency error and OOS measurement subnetwork.

The subnetwork is in compliance with measurement specifications described in GSM 11.10, version 8.1.0, release 1999, and Option 202 of the Agilent E4406A VSA.



EDGE_FreqErr_OffsetSupp_Meas Schematic

Reference data passes through the upper path and is input to the EDGE_FrequencyErr subnetwork; test data passes through the lower path to the EDGE_FrequencyErr subnetwork, which performs the core frequency error and OOS calculations.

The Chop component is used to select the burst that will be tested from a frame. It also selects the useful-part symbols in that burst; all other symbols are discarded. The burst (time slot) to be measured is specified by the TS_Measured parameter.

Test results of frequency error and origin offset suppression are determined over multiple bursts; TS_Num indicates the number of bursts to be measured and averaged.

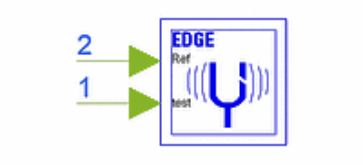
The Delay component inserts a 1-symbol delay in the test data path to ensure the test path is delayed for the measurement.

For details and formulas regarding frequency error and OOS calculation, refer to the EDGE_FrequencyErr documentation.

References

1. Tdoc SMG7 022/00 version 420, CR 11.10, Introduction of EGPRS Transmitter Tests for Frequency Error, Power, ORFS and Intermodulation Attenuation, 13.17.1, March 22-24, 2000.
2. ETSI SMG2 EDGE Tdoc 370r1/99, Modulation accuracy for EDGE MS and BTS, August 24-27, Paris, France, 1999.
3. GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 8.3.0, Release 1999.
4. GSM 05.10, Radio subsystem synchronization, version 3.5.1, October 1992.

EDGE_FrequencyErr



Description Frequency error measurement with reference signal input
Library EDGE, Measurement
Class SDFEDGE_FrequencyErr

Parameters

Name	Description	Default	Unit	Type	Range
StartSym	start symbol	142		int	[0, ∞)
SymBurstLen	number of symbols within burst to be measured	142		int	[1, 10000]
SampPerSym	number of samples per symbol	16		int	[1, ∞)
SymDelayBound	upper bound of delay detection, in symbol, -1 for no detection	3		int	[-1, ∞)†
NumBursts	number of bursts to be measured	5		int	[1, ∞)††
MeasType	type of measurement: frequency error, origin offset suppression	frequency error		enum	
SymbolRate	symbol rate	(1625/6) kHz	Hz	real	(0, ∞)†††

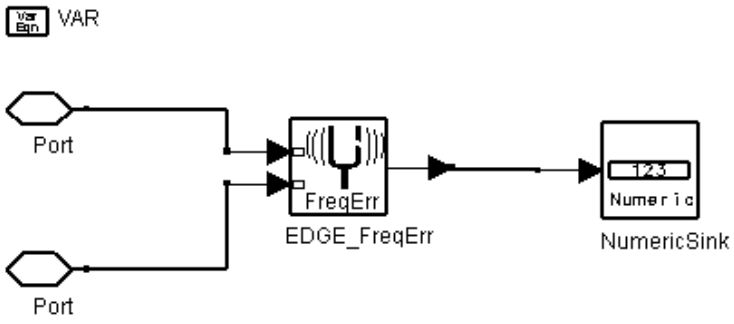
† The model fulfills the synchronization (detects the delay of test signals, and aligns them with the reference signals) inside this boundary. If set to -1, synchronization will not be applied.†† Measurement results are determined over multiple bursts; NumBursts indicates the number of bursts to be measured and averaged. ††† SymbolRate is used to calculate the frequency error; the default value 270.833 kHz is the symbol rate of EDGE/GSM.

Pin Inputs

Pin	Name	Description	Signal Type
1	testDataInput	signals to be measured	complex
2	RefDataInput	reference signals	complex

Notes/Equations

1. This subnetwork is used to measure the frequency error and origin offset suppression (OOS) for communication systems such as EDGE. The subnetwork wraps EDGE_FreqErr and a numeric sink to function as a sink. EDGE_FreqErr is derived from EDGE_EVM_WithRefIn, which is used to measure EVM.



EDGE_FrequencyErr Schematic

2. Frequency error and OOS, as well as the EVM, are evaluations of modulation accuracy.
   This design test is implemented according to the methods and requirements described in 13.17.1 of GSM 11.10 and corresponding *Change Request* .
   Frequency error and OOS are defined as follows.
   The transmitted signal is modeled by:

   Y(t) = C1{R(t) + D(t) + C0}Wt

   where

   R(t) is defined to be an ideal transmitter signal (reference signal)

   D(t) is the residual complex error on signal R(t)

   C0 is a constant origin offset representing carrier feed-through

   C1 is a complex constant representing the arbitrary phase and output power of the transmitter

   W = $e^{\alpha + j2\pi f}$ accounts for both a frequency offset of 2πf radians per second phase rotation and an amplitude change of α nepers per second

   The symbol timing phase of Y(t) is aligned with R(t).
   The transmitted signal Y(t) is compensated in amplitude, frequency and phase by

multiplying by the factor:

$W^{-t}/C1$

Values for W and C1 are determined using an iterative procedure. W(α,f), C1 and C0 are chosen to minimize the RMS value of EVM.
After compensation, Y(t) is passed through the specified measurement filter (GSM 05.05, 4.6.2) to produce the signal

$Z(k) = S(k) + E(k) + C0$

where

S(k) is the ideal transmitter signal observed through the measurement filter

k = floor(t/T_s), where T_s =1/270.833kHz corresponding to the symbol times

The frequency error is defined as the f of W = $e^{\alpha + j2\pi f}$.
The OOS is defined as

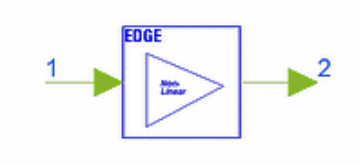
$$OOS(dB) = -10\log_{10}\left(\frac{|C_0|^2}{\frac{1}{N}\sum_{k\in K}|S(k)|^2}\right)$$

3. The EDGE_FreqErr model in this sub-network is derived from EDGE_EVM_WithRefIn. So, the parameter setting for this subnetwork is similar to that for EVM subnetwork. Algorithms used to estimate W, C1 and C0 in the calculation of frequency error and OOS are identical to those of the EVM calculation.

References

1. 13.17.1 of GSM 11.10-1 version 8.1.0 Release 1999
2. ETSI Tdoc SMG7 022/00, CR 11.10, Introduction of EGPRS Transmitter Tests for Frequency Error, Power, ORFS and Intermodulation Attenuation, March 22-24, 2000.

EDGE_NonLinearAmp



Description Non-linear power amplifier
Library EDGE, Measurement
Class SDFEDGE_NonLinearAmp

Parameters

Name	Description	Default	Type	Range
InputNormValue	input normalization value, in dBw	0	real	†
OutputNormValue	output normalization value, in dBw	0	real	†
InputType	input signal type: Absolute Value, Normalized Value	Absolute Value	enum	
† if InputType is Absolute Value, InputNormValue and OutputNormValue will be used to normalize the input and output signals so that (0,0) corresponds to 1dB compression point intervals				

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input signal	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output signal	complex

Notes/Equations

1. This model is used to provide a reference for nonlinear amplifiers for use in the derivation of performance specifications for EDGE terminals.
   The device is considered memoryless. Individual fits are made to the amplitude and phase transfer characteristics. The amplitude transfer has the form

$$P_0 = -10\log\left(1+10^{\frac{d-x}{10}}\right)+\left(\exp\left(-\frac{(x-b)^2}{c}\right)\right)^f+g$$

   where

$$x = P_{in}-e$$

   P_{in} and P_o are the input and output powers, in dB. They are normalized such that (0,0) corresponds to the 1dB compression point
   b = −0.0005
   c = 0.34
   d = −0.9
   e = 3.55
   f = 0.005
   g = 3.7
   The phase transfer is modelled as

$$\Delta\varphi = \alpha\exp\left(-\frac{P_{in}}{\beta}\right)+\gamma\exp\left(-\frac{P_{in}}{\delta}\right)$$

   where
   Δφ is in degrees
   P_{in} is the input power in dB (relative to the 1 dB compression point)
   α = 100
   β = −5.05
   γ = −96.5
   δ = −5
   The characteristic is normalized to an AM/PM coefficient of 0.5°/dB at a 1 dB compression point.

References

1. ETSI TDOC SMG2 EDGE 2E99-017, Reference Models for Nonlinear Amplifiers and Phase Noise for Evaluation of EDGE Radio Performance, Toulouse, France, 2-4 March, 1999.

EDGE_Pwr_Meas

Description VSA compatible mean transmitted RF carrier power measurement
Library EDGE, Measurement
Class TSDFEDGE_Pwr_Meas

Parameters

Name	Description	Default	Unit	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
FCarrier	carrier frequency	890.2e6	Hz	real	(0, ∞)
TS_Measured	time slot to be measured	0		int	[0, 7]
RIn	input resistance	50.0 Ohm	Ohm	real	[0, ∞)
RTemp	resistor physical temperature	-273.15		real	(-∞, ∞)

Pin Inputs

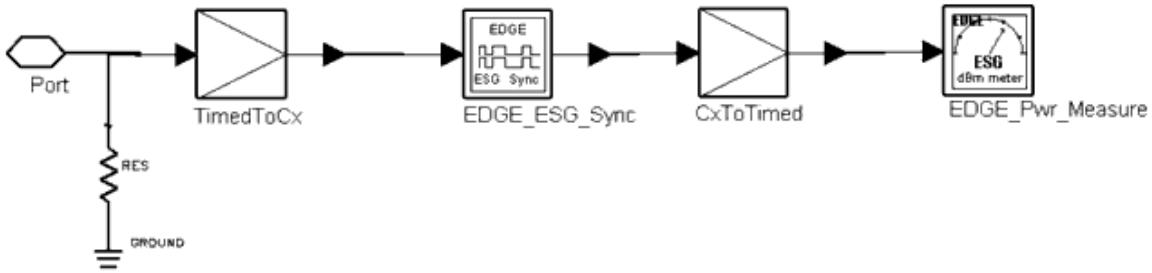
Pin	Name	Description	Signal Type
1	input	RF input	timed

Notes/Equations

This subnetwork is used to measure the mean transmitted RF carrier power. The schematic for the subnetwork is shown in the following figure.

The signal to be measured must have the frame structure specified in GSM 05.02, version 8.3.0, Release 1999. That is, the first and the fifth bursts in one TDMA frame each contain 157 symbols while the others contain 156 symbols.

EDGE_ESG_Sync synchronizes the input framed signal; EDGE_Pwr_Measure then measures the mean power of the input signal.



EDGE_Pwr_Meas Schematic

References

1. 13.17.3 of ETSI Tdoc SMG7 022/00, version 420, CR 11.10 Introduction of EGPRS Transmitter Tests for Frequency Error, Power, ORFS and Intermodulation Attenuation, March 22-24, 2000.
2. GSM 05.02, version 8.3.0, Release 1999.

EDGE_Pwr_vs_Time_Meas

Description VSA compatible power vs time measurement for EDGE
Library EDGE, Measurement
Class TSDFEDGE_Pwr_vs_Time_Meas

Parameters

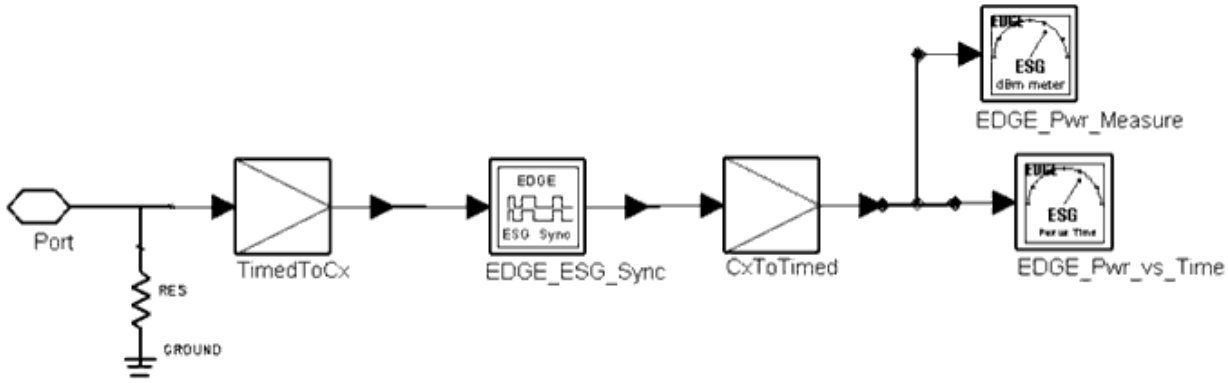
Name	Description	Default	Unit	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
FCarrier	carrier frequency	890.2e6	Hz	real	(0, ∞)
TS_Measured	time slot to be measured in each TDMA frame,0 to 7.	0		int	[0, 7]
RIn	input resistance	50.0 Ohm	Ohm	real	[0, ∞)
RTemp	resistor physical temperature	-273.15		real	(-∞, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input RF data to be measured	timed

Notes/Equations

1. This subnetwork is used to measure the transmitted RF carrier power versus time of the input signal. The schematic is shown in the following figure.
   In the input signal, the first and the fifth bursts in one TDMA frame must contain 157 symbols while the other bursts contain 156 symbols, as specified in GSM 05.02, version 8.3.0, Release 1999.
2. EDGE_ESG_Sync synchronizes the input framed signal. EDGE_Pwr_Measure measures the mean power of the input signal for normalization purposes. EDGE_Pwr_vs_Time then measures power versus time.



EDGE_Pwr_vs_Time_Meas Schematic

References

1. 13.17.3 of ETSI Tdoc SMG7 022/00, version 420, CR 11.10 Introduction of EGPRS Transmitter Tests for Frequency Error, Power, ORFS and Intermodulation Attenuation, March 22-24, 2000.
2. GSM 05.02, version 8.3.0, Release 1999.

EDGE_RCWindow_RCFilter

Description Raised-cosine windowed raised-cosine filter
Library EDGE, Measurement
Class SDFEDGE_RCWindow_RCFilter

Parameters

Name	Description	Default	Sym	Type	Range
Interpolation	interpolation ratio	16	I	int	[1, ∞)†
SampPerSym	number of samples per symbol	16	S	int	[1, ∞)
† I-1 zeros are inserted after each input data before filtering; this makes an I-ratio interpolation.					

Pin Inputs

Pin	Name	Description	Signal Type
1	input	data to be filtered	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	output	filtered data	complex

Notes/Equations

1. This model fulfills the raised-cosine windowed raised-cosine FIR filtering, and is used as the EDGE measurement filter, especially for EVM. Each firing, one token is consumed at input and I tokens are produced at output.
   The RC-windowed RC filter (proposed by Agilent Technologies in [1]) used in this model is obtained by windowing the impulse response of the original RC filter using a raised-cosine window. As a result, this RC-windowed RC filter eliminates problems of the former RC filter and has an acceptable out-of-band (beyond 188 kHz) rejection. Previous RC measurement filters caused EVM measurement errors because it allowed symbols beyond the useful part of a burst to influence the values of EVM within the measurement interval. And, the length of the impulse response was not defined, which allowed different lengths in different measurement instruments and lead to different measurement results. Defining the truncation length of that measurement filter to be equal to five symbol intervals eliminates these problems. However, out-of-band rejection of the short RC filter is poor, and the noise bandwidth increases significantly.
   This filter retains the bandpass characteristics of the former RC filter and involves the smallest departure from it, which avoids the invalidation of the simulation results that have been obtained using the former RC filter. The only disadvantage of the RC-windowed RC filter is poor adjacent channel rejection.
2. Characteristics of the RC-windowed RC filter are:

   Bandwidth (6dB): 90 kHz

   Rolloff Factor: 0.25

   Impulse Response Length: 7.5 T

   where T is the symbol interval. A non-causal impulse response is considered for simplification.

   RC window:

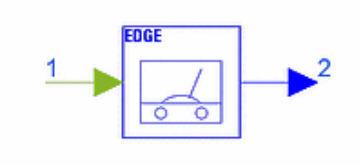
$$winRC = \begin{cases} 1, & 0 \le |t| \le 1.5T \\ 0.5\left(1 + \cos\left[\pi\frac{(|t| - 1.5T)}{2.25T}\right]\right), & 1.5T \le |t| \le 3.75T \\ 0, & |t| \le 3.75T \end{cases}$$

References

1. ETSI SMG2 WS #11, Tdoc SMG2 2e99-459, A New Measurement Filter for EDGE,

Austin, Texas, October 18-22, 1999.

EDGE_SigPowerMeasure



Description Average signal power measurement
Library EDGE, Measurement
Class SDFEDGE_SigPowerMeasure

Parameters

Name	Description	Default	Sym	Type	Range
BurstType	burst type: Normal Burst, Synchronization Burst, Access Burst	Normal Burst		enum	
SampPerSym	number of samples per symbol	8	N	int	(0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input over-sampled signal	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	output	average power of signal	real

Notes/Equations

1. This model is used to measure the average signal power at the receiving part in system link tests.
   Each firing, one token is produced at output when 156 × N tokens are consumed at input, where N is the number of samples per symbol.
   Output units are joules/sample.
2. Signal-to-noise ratio (SNR) is one of the most common conditions in system link simulation. The power of additive white Gaussian noise (AWGN) can be set according to signal power to obtain a certain SNR.
3. This model is used to measure baseband signal power. (To measure RF signal power, use EDGE_PwrMeasure or EDGE_Pwr_vs_Time, which can measure baseband and RF signals.)
   The equation of signal power measurement is

$$P_s = \frac{1}{N}\sum_{n=0}^{N-1}|S_n|^2$$

   where

$N = (156 - N_G) \times N_B \times N_S$ is the total number of samples measured

   N_G is the number of guard symbols in a burst

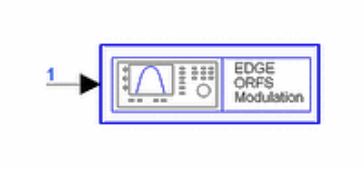
   N_B is the number of bursts measured

   N_S is the number of samples per symbol

   S_n is the sample of input signal

   Guard symbols are ignored in signal power measurement.

EDGE_TxORFS_Modulation_Meas



Description VSA compatible ORFS measurement due to modulation
Library EDGE, Measurement
Class TSDFEDGE_TxORFS_Modulation_Meas

Parameters

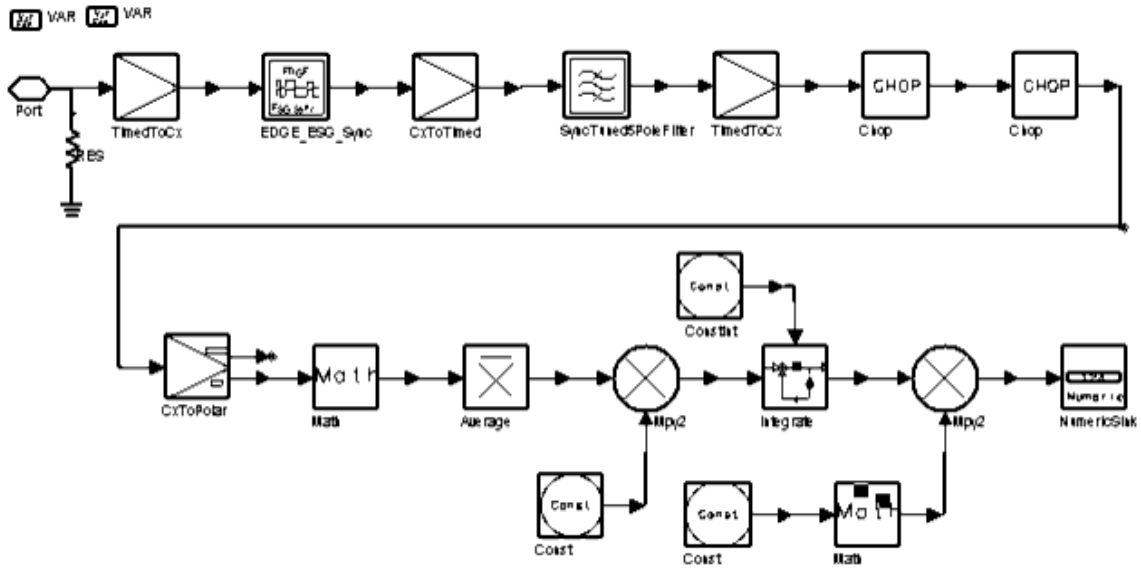
Name	Description	Default	Unit	Type	Range
SampPerSym	number of samples per symbol	16		int	[1, ∞)
FCarrier	carrier frequency	890.2e6	Hz	real	(0, ∞)
TS_Num	number of time slots measured	50		int	[1, ∞)
TS_Measured	time slot to be measured in each TDMA frame,0 to 7.	0		int	
RIn	input resistance	50.0 Ohm	Ohm	real	[0, ∞)
RTemp	resistor physical temperature	-273.15		real	(-∞, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	RF_in	RF input	timed

Notes/Equations

1. This subnetwork is used to measure the output RF spectrum due to modulation. The schematic is shown in the following figure.
   In the input signal to be measured the first and the fifth bursts in one TDMA frame must contain 157 symbols while other bursts contain 156 symbols (as specified in GSM 05.02, version 8.3.0, Release 1999).
2. Before the output RF spectrum is measured, EDGE_ESG_Sync synchronizes the input framed signal. The synchronized signal passes through SyncTuned5PoleFilter. This is a cascade of five bandpass first-order Butterworth filters. All five filters are centered at FCarrier and have the same 3 dB bandwidth. The resulting filter is also centered at FCarrier and has a 3 dB bandwidth of 30 kHz. By sweeping the center frequency of this filter at 30 kHz steps a filter bank is implemented that can spectrally split the input signal into 30 kHz channels.
   The time domain signal corresponding to each one of these channels is gated to extract a segment of 40 symbols from the useful part of each time slot. The mean signal power over all these gated segments is then exported as the value of the spectrum at FCarrier frequency.



EDGE_TxORFS_Modulation_Meas Schematic

References

1. 13.4 of GSM 11.21, version 7.1.0, Release 1998.

2. 13.17.4 of ETSI Tdoc SMG7 022/00, version 420, CR 11.10 Introduction of EGPRS Transmitter Tests for frEquency Error, Power, ORFS and Intermodulation Attenuation, March 22-24, 2000.
3. GSM 05.02, version 8.3.0, Release 1999.

EDGE_TxORFS_Switching_Meas

Description VSA compatible ORFS measurement due to switching
Library EDGE, Measurement
Class TSDFEDGE_TxORFS_Switching_Meas

Parameters

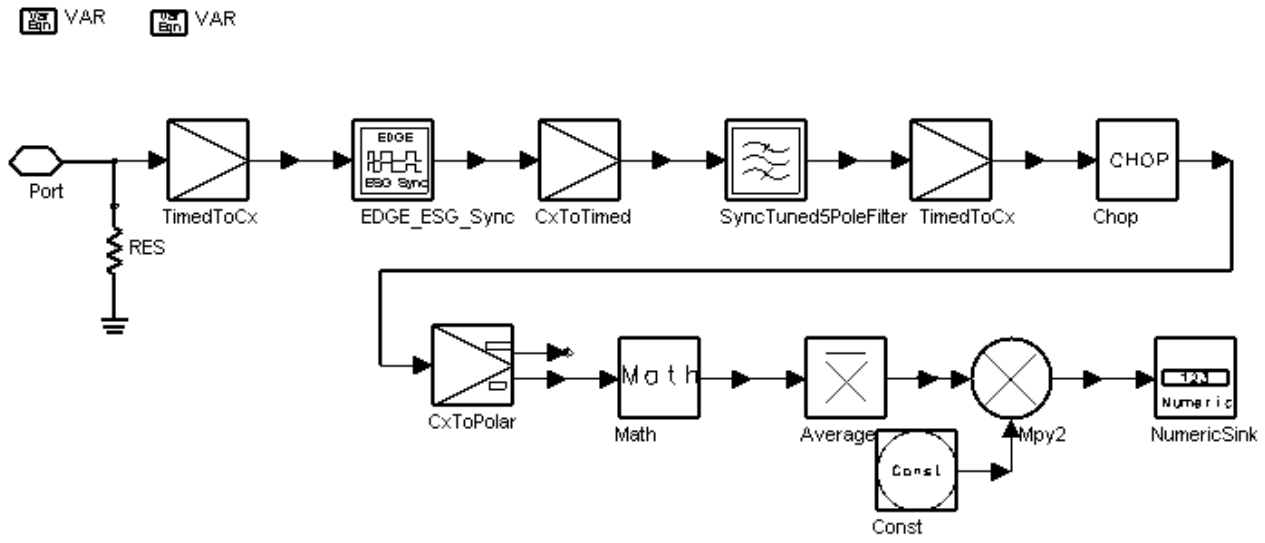
Name	Description	Default	Unit	Type	Range
SampPerSym	number of samples per symbol	16		int	[1, ∞)
FCarrier	carrier frequency	890.2e6	Hz	real	(0, ∞)
TS_Num	number of time slots measured	50		int	[1, ∞)
TS_Measured	time slot to be measured in each TDMA frame,0 to 7.	0		int	
RIn	input resistance	50.0 Ohm	Ohm	real	[0, ∞)
RTemp	resistor physical temperature	-273.15		real	(-∞, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	RF_in	RF input	timed

Notes/Equations

1. This subnetwork is used to measure the output RF spectrum due to switching, which is the relationship between the frequency offset from the carrier and the power, measured in a specified bandwidth and time, produced by the transmitter due to the effect of power ramping. The schematic for the subnetwork is shown in the following figure.
   In the input signal to be measured, the first and the fifth bursts in each TDMA frame must contain 157 symbols while the other bursts contain 156 symbols (as specified in GSM 05.02, version 8.3.0, Release 1999).



EDGE_TxORFS_Switching_Meas Schematic

2. Before the output RF spectrum is measured, EDGE_ESG_Sync synchronizes the input framed signal. The synchronized signal passes through SyncTuned5PoleFilter. This is a cascade of five bandpass first-order Butterworth filters. All five filters are centered at FCarrier and have the same 3 dB bandwidth. The resulting filter is also centered at FCarrier and has a 3 dB bandwidth of 30kHz. By sweeping the center frequency of this filter at 30 kHz steps a filter bank is implemented that can spectrally split the input signal into 30 kHz channels.
   The time domain signal corresponding to each one of these channels is gated to extract the segment of 148 symbols of the useful part of each time slot. The mean signal power over TS_Num gated segments is then exported as the value of the spectrum at FCarrier frequency.

References

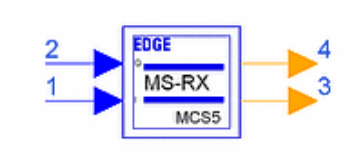
1. 13.4 of GSM 11.21, version 7.1.0, Release 1998.

2. 13.17.4 of ETSI Tdoc SMG7 022/00, version 420, CR 11.10 Introduction of EGPRS Transmitter Tests for Frequency Error, Power, ORFS and Intermodulation Attenuation, March 22-24, 2000.
3. GSM 05.02, version 8.3.0, Release 1999.

Mobile Station Test and Verification Components

- *EDGE MS MCS5 Receiver* (edge)
- *EDGE MS MCS6 Receiver* (edge)
- *EDGE MS MCS7 Receiver* (edge)
- *EDGE MS MCS8 Receiver* (edge)
- *EDGE MS MCS9 Receiver* (edge)
- *EDGE MultipathDown* (edge)

EDGE_MS_MCS5_Receiver



Description EDGE MS MCS5 receiver
Library EDGE, MS Test and Verification
Class SDFEDGE_MS_MCS5_Receiver

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_Measured	time slot measured	0		int	[0, 7]
TSC	training sequence code	0		int	[0, 7]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†
† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$, Ji is the number of states on stage i, $1 \le i \le L$					

Pin Inputs

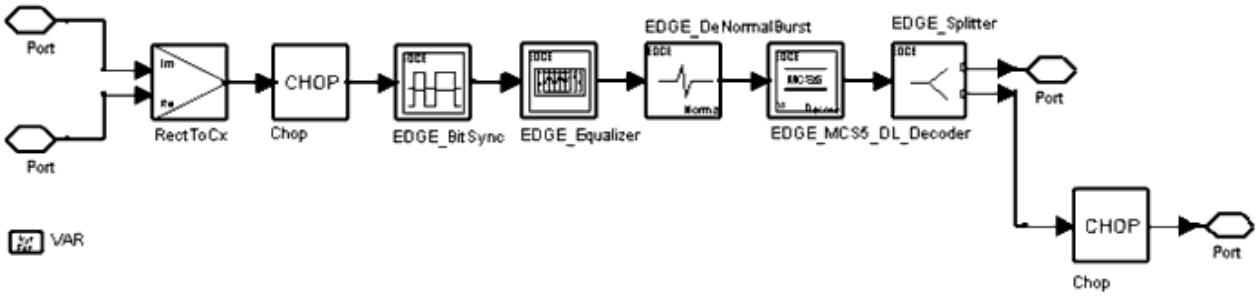
Pin	Name	Description	Signal Type
1	I	inphase input	real
2	Q	quadrature input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	USF	USF output	int
4	Data	data output	int

Notes/Equations

1. This subnetwork is used to demodulate and decode the downlink baseband signal of coding scheme MCS5.
2. The schematic for this subnetwork is shown in the following figure. It consists of EDGE_BitSync, EDGE_Equalizer, EDGE_DeNormalBurst, EDGE_MCS5_DL_Decoder, EDGE_splitter, and two Chop components. The first Chop extracts the measured slots from the input frames; EDGE_Splitter separates data bits from the USF bits and header bits; the second Chop extracts the USF bits.

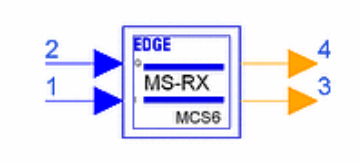


EDGE_MS_MCS5_Receiver Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MS_MCS6_Receiver



Description EDGE MS MCS6 receiver
Library EDGE, MS Test and Verification
Class SDFEDGE_MS_MCS6_Receiver

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_Measured	time slot measured	0		int	[0, 7]
TSC	training sequence code	0		int	[0, 7]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†

† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$, Ji is the number of states on stage i, $1 \le i \le L$

Pin Inputs

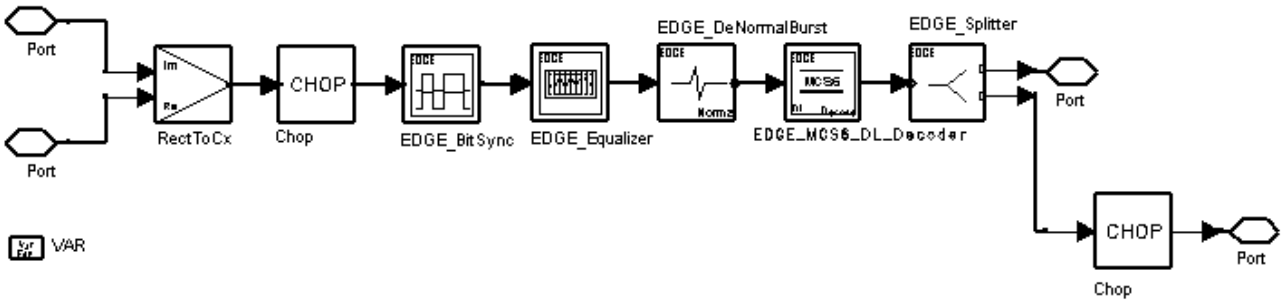
Pin	Name	Description	Signal Type
1	I	inphase input	real
2	Q	quadrature input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	USF	USF output	int
4	Data	data output	int

Notes/Equations

1. This subnetwork is used to demodulate and decode the downlink baseband signal of coding scheme MCS6.
2. The schematic for this subnetwork is shown in the following figure. It consists of EDGE_BitSync, EDGE_Equalizer, EDGE_DeNormalBurst, EDGE_MCS6_DL_Decoder, EDGE_Splitter, and two Chop components. The first Chop extracts the measured slots from the input frames; EDGE_Splitter separates data bits from the USF bits and header bits; the second Chop extracts the USF bits.

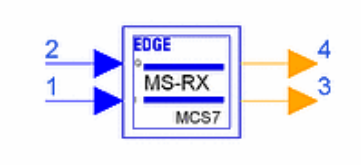


EDGE_MS_MCS6_Receiver Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MS_MCS7_Receiver



Description EDGE MS MCS7 receiver
Library EDGE, MS Test and Verification
Class SDFEDGE_MS_MCS7_Receiver

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_Measured	time slot measured	0		int	[0, 7]
TSC	training sequence code	0		int	[0, 7]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†

† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$, Ji is the number of states on stage i, $1 \le i \le L$.

Pin Inputs

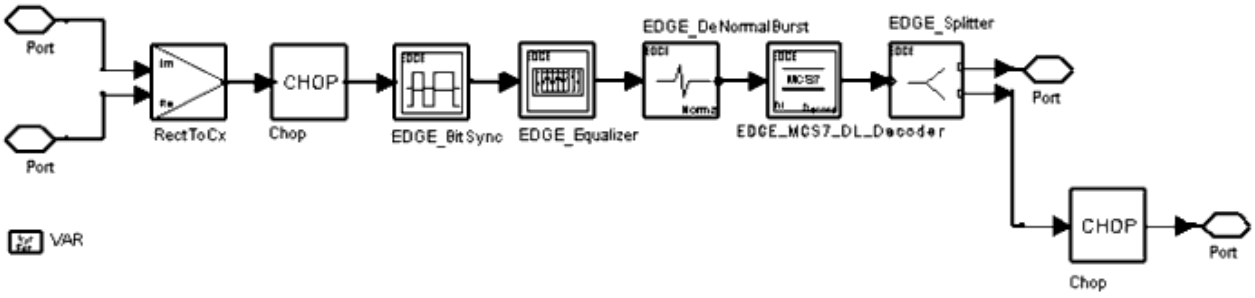
Pin	Name	Description	Signal Type
1	I	inphase input	real
2	Q	quadrature input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	USF	USF output	int
4	Data	data output	int

Notes/Equations

1. This subnetwork is used to demodulate and decode the downlink baseband signal of coding scheme MCS7.
2. The schematic for this subnetwork is shown in the following figure. It consists of EDGE_BitSync, EDGE_Equalizer, EDGE_DeNormalBurst, EDGE_MCS7_DL_Decoder, EDGE_splitter, and two Chop components. The first Chop extracts measured slots from the input frames; EDGE_Splitter separates data bits from the USF bits and header bits; the second Chop extracts the USF bits.

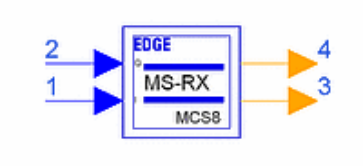


EDGE_MS_MCS7_Receiver Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MS_MCS8_Receiver



Description EDGE MS MCS8 receiver
Library EDGE, MS Test and Verification
Class SDFEDGE_MS_MCS8_Receiver

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_Measured	time slot measured	0		int	[0, 7]
TSC	training sequence code	0		int	[0, 7]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†

† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le 8$, Ji is the number of states on stage i, $1 \le i \le L$

Pin Inputs

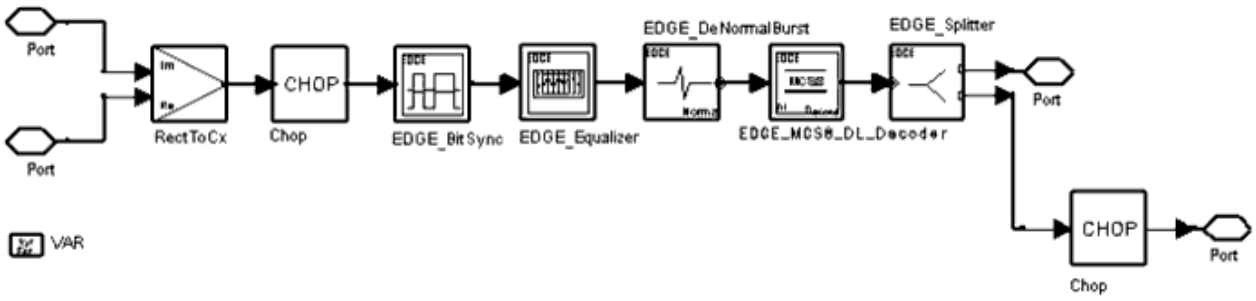
Pin	Name	Description	Signal Type
1	I	inphase input	real
2	Q	quadrature input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	USF	USF output	int
4	Data	data output	int

Notes/Equations

1. This subnetwork is used to demodulate and decode the downlink baseband signal of coding scheme MCS8.
2. The schematic for this subnetwork is shown in the following figure. It consists of EDGE_BitSync, EDGE_Equalizer, EDGE_DeNormalBurst, EDGE_MCS8_DL_Decoder, EDGE_splitter, and two Chop components. The first Chop extracts measured slots from the input frames; EDGE_Splitter separates data bits from the USF bits and header bits; the second Chop extracts the USF bits.

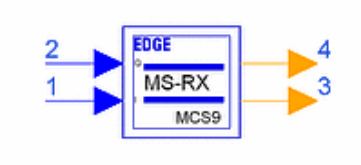


EDGE_MS_MCS8_Receiver Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MS_MCS9_Receiver



Description EDGE MS MCS9 receiver
Library EDGE, MS Test and Verification
Class SDFEDGE_MS_MCS9_Receiver

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_Measured	time slot measured	0		int	[0, 7]
TSC	training sequence code	0		int	[0, 7]
Algorithm	equalization algorithm: MLSE, RSSE	RSSE		enum	
MaxDelay	maximum delay of channel in symbol duration units	5	L	int	[1, 5]
PartitionArray	array of number of subsets used in each stage of RSSE	8 4 2 1 1		int array	†

† PartitionArray is valid only when Algorithm = RSSE. All PartitionArray elements must be a power of 2, and $1 \le J_L \le J_{L-1} \le \ldots \le J_1 \le$, Ji is the number of states on stage i, $1 \le i \le L$

Pin Inputs

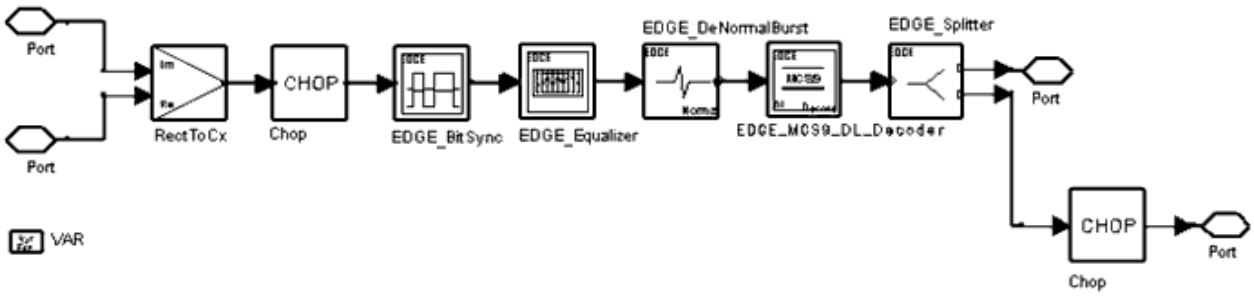
Pin	Name	Description	Signal Type
1	I	inphase input	real
2	Q	quadrature input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	USF	USF output	int
4	Data	data output	int

Notes/Equations

1. This subnetwork is used to demodulate and decode the downlink baseband signal of coding scheme MCS9.
2. The schematic for this subnetwork is shown in the following figure. It consists of EDGE_BitSync, EDGE_Equalizer, EDGE_DeNormalBurst, EDGE_MCS9_DL_Decoder, EDGE_Splitter, and two Chop components. The first Chop component extracts measured slots from the input frames; EDGE_Splitter separates data bits from the USF bits and header bits; the second Chop extracts the USF bits.

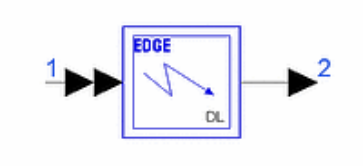


EDGE_MS_MCS9_Receiver Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MultipathDown



Description Downlink multipath simulator for EDGE
Library EDGE, MS Test and Verification
Class TSDFEDGE_MultipathDown

Parameters

Name	Description	Default	Unit	Type	Range
Type	GSM type options: NoMultipath, RuralArea1, RuralArea2, HillyTerrain6Tap1, HillyTerrain6Tap2, HillyTerrain12Tap1, HillyTerrain12Tap2, UrbanArea6Tap1, UrbanArea6Tap2, UrbanArea12Tap1, UrbanArea12Tap2, EqualizationTest	NoMultipath		enum	
Pathloss	inclusion of large-scale pathloss: No, Yes	No		enum	
Seed	integer number to randomize the channel output	1234567		int	[1, ∞)
X	X-position coordinate of mobile antenna	100.0 meter	m	real	(-∞, ∞)
Y	Y-position coordinate of mobile antenna	0.0 meter	m	real	(-∞, ∞)
SpeedType	velocity unit option: km/hr, miles/hr	km/hr		enum	
Vx	X component of velocity vector	0.0		real	[0, ∞)
Vy	Y component of velocity vector	0.0		real	[0, ∞)

Pin Inputs

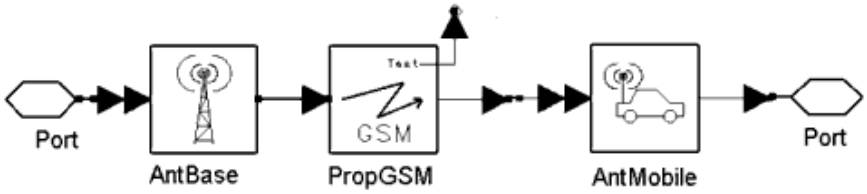
Pin	Name	Description	Signal Type
1	input	input RF signal	multiple timed

Pin Outputs

Pin	Name	Description	Signal Type
2	output	input RF signal	timed

Notes/Equations

1. This subnetwork is used to simulate the downlink multipath channel for EDGE.
2. The schematic for this subnetwork is shown in the following figure. It consists of AntBase, PropGSM, and AntMobile, to simulate the base station antenna, channel propagation condition, and the mobile station antenna, respectively.

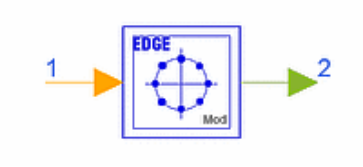


EDGE_MultipathDown Schematic

Modems for EDGE Design Library

- *EDGE 8PSKMod* (edge)
- *EDGE PhaseRotator* (edge)
- *EDGE PulseShapingFltr* (edge)
- *EDGE RxFilter* (edge)

EDGE_8PSKMod



Description Generation of 8PSK modulated signal
Library EDGE, Modems
Class SDFEDGE_8PSKMod

Parameters

Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	(0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input bits, taking the value of 0 or 1	int

Pin Outputs

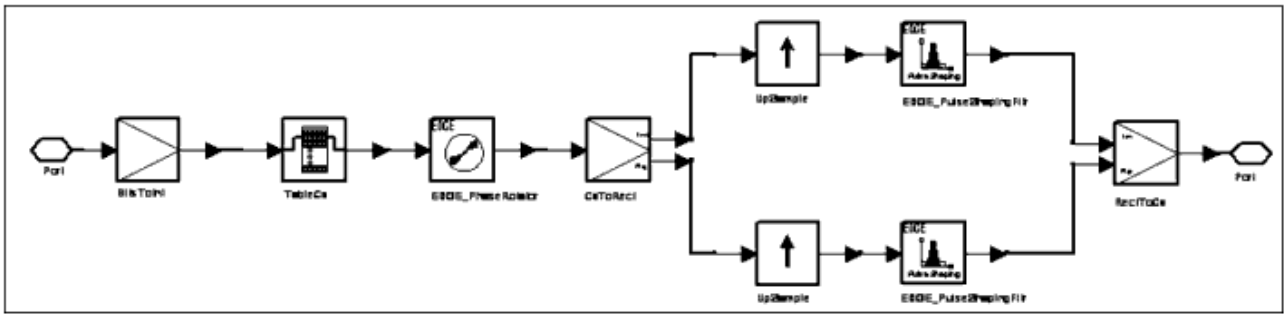
Pin	Name	Description	Signal Type
2	output	complex envelope of modulated signal.	complex

Notes/Equations

1. This subnetwork generates the complex envelope of 8PSK modulated signals.
2. The schematic for this subnetwork is shown in the following figure.
   The input bits are mapped to the 8PSK constellation, three bits a symbol (by BitsToInt and TableCx). The mapped symbols are represented by complex numbers that depict the coordinates in the 8PSK constellation. EDGE_PhaseRotator generates a complex symbol sequence:

$$\left\{ e^{j0}, e^{j\frac{3}{8}\pi}, e^{j\frac{6}{8}\pi}, e^{j\frac{9}{8}\pi}, \ldots \right\}$$

   This sequence is multiplied into mapped symbols, thereby implementing the continuous $\frac{3}{8}\pi$ phase rotation. Phase rotation prevents the phase trajectories from going through the origin which causes the envelope of modulated signals to become zero.
   After phase rotation, the complex symbols are split into real and imaginary routes, up-sampled and pulse-shaped in both routes. Then the symbols are transformed back to complex by merging the two routes; these complex symbols are the output of this subnetwork.

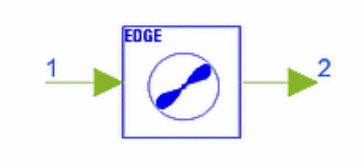


EDGE_8PSKMod Schematic

References

1. ETSI Tdoc SMG2 WPB 108/98, Ericsson, EDGE Evaluation of 8-PSK

EDGE_PhaseRotator



Description Phase rotator used in 8PSK modulation
Library EDGE, Modems
Class SDFEDGE_PhaseRotator

Pin Inputs

Pin	Name	Description	Signal Type
1	input	input data sequence	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output data sequence	complex

Notes/Equations

1. This model is used to implement a cumulative $\frac{3}{8}\pi$ phase rotation to the input symbol, which is one feature of the modified 8PSK modulation used in EDGE systems. Each firing, one output token is produced when one input token is consumed.
2. Operation of this model can be expressed by the equation

   $$S_{out} = S_{in} \times e^{\theta}$$

   where

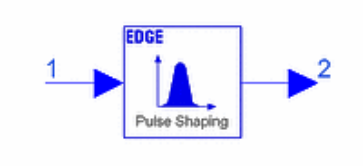
   $$\theta = n \times \frac{3}{8}\pi \mod 2\pi$$

   n is a counter starting from 0 to count the number of symbols.

References

1. ETSI Tdoc SMG2 WPB 108/98, Ericsson, EDGE Evaluation of 8-PSK.

EDGE_PulseShapingFltr



Description Pulse shaping filter
Library EDGE, Modems
Class SDFEDGE_PulseShapingFltr

Parameters

Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	(0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	input	data to be pulse shaped	real

Pin Outputs

Pin	Name	Description	Signal Type
2	output	pulse shaped data	real

Notes/Equations

This model is the modulation pulse shaping filter; it is used to control the power of the spectrum outband and decrease the peak-to-average ratio.

Each firing, one token is consumed at input and one token is produced at output.

The impulse response of this filter is C_0 (t), which is the main component in the Laurent expansion of the GMSK modulation. In his paper[1], Laurent introduces a method to express any constant-amplitude binary phase modulation as a sum of a finite number of time-limited amplitude-modulated pulses (AMP decomposition). Using this method in GMSK, which is a constant-amplitude phase modulation, the GMSK signals can be transformed into the sum of C_0 (t), C_1 (t), ... , C_M (t), where M is derived from the length of the impulse response of the Gaussian filter. And, compared to C_0 (t), other components C_1 (t), ... , C_M (t) are all negligible.

C_0 (t) is defined in the following equations.

$$C_0(t) = \begin{cases} \prod_{i=0}^{5} S_i(t) & 0 \le t \le 5T \\ 0 & \text{else where} \end{cases}$$

where

$$S_i(t) = S_0(t + iT)$$

and

$$S_0(t) = \begin{cases} \sin\left(\pi \int_{-\infty}^{t} g(\tau)d\tau\right) & 0 \le t \le 4T \\ \sin\left(\frac{\pi}{2} - \pi \int_{-\infty}^{t-4T} g(\tau)d\tau\right) & 4T \le t \le 8T \\ 0 & \text{else where} \end{cases}$$

where, g(t) is the rectangular pulse response of the Gaussian filter in GMSK modulation.

$$g(t) = \frac{1}{2T}\left(Q\left(2\pi \times 0.3\frac{t - \frac{5T}{2}}{T\sqrt{\ln(2)}}\right) - Q\left(2\pi \times 0.3\frac{t - \frac{3T}{2}}{T\sqrt{\ln(2)}}\right)\right)$$

and

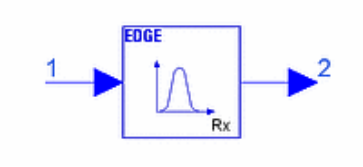
$$Q(t) = \frac{1}{\sqrt{2\pi}} \int_{t}^{\infty} e^{-\frac{\tau^2}{2}} d\tau$$

and T is the symbol period.

References

1. P. A. Laurent, "Exact and Approximate Construction of Digital Phase Modulations by Superposition of Amplitude Modulated Pulses (AMP)," *IEEE Trans. Commun* ., vol. COM-34, NO. 2, pp. 150-160, Feb. 1986.
2. P. Qinhua, G. Yong and L. Weidong, "Synchronization Design Theory of Demodulation for Digital Land Mobile Radio System," *Journal of Beijing University of Posts and Telecommunications* , Vol. 18, No. 2, pp. 14-21, Jun. 1995.
3. ETSI Tdoc SMG2 WPB 108/98, Ericsson, EDGE Evaluation of 8-PSK.

EDGE_RxFilter



Description Receiving filter for EVM measurement
Library EDGE, Modems
Class SDFEDGE_RxFilter

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	16	M	int	(0, ∞)
IRLength	length of filter impulse response, in sample	240	R	int	††
† R should be set to odd times of M. The transmitting filter impulse response is 5 symbol periods. So only when the response length of this filter is also an odd number of symbol periods can the total delay of the system (in which both filters are used) make sense.					

Pin Inputs

Pin	Name	Description	Signal Type
1	input	base band modulated data	real

Pin Outputs

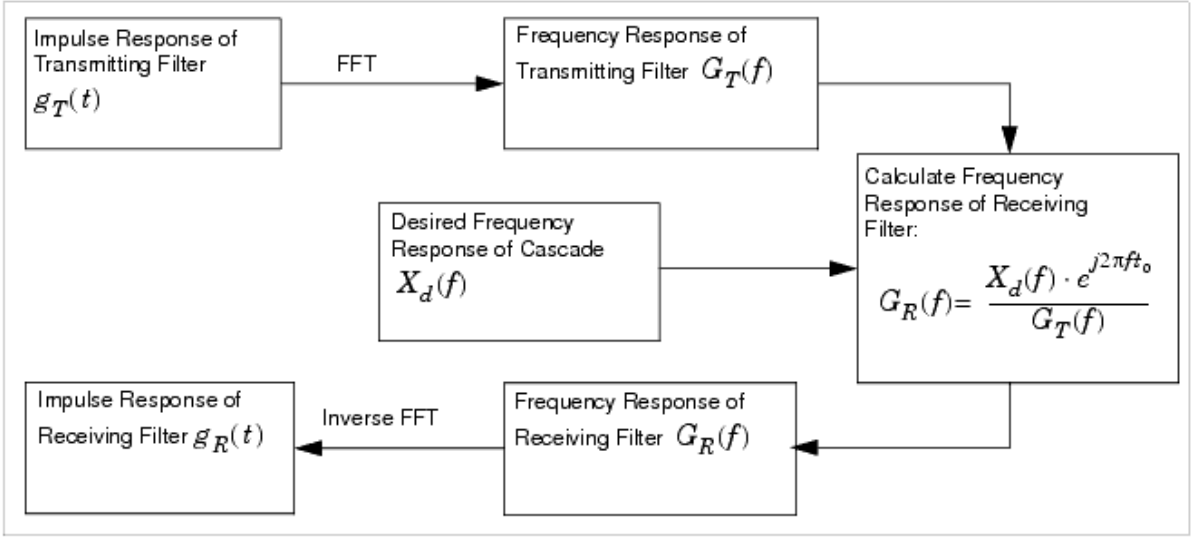
Pin	Name	Description	Signal Type
2	output	filtered data	real

Notes/Equations

1. This receiving filter is used to control the inter-symbol interference (ISI) of the transmitted symbols, so a simplified coherent symbol-by-symbol demodulation can be accomplished. From this demodulation, the original transmitted symbols can be recovered; then the EVM measurement reference signals can be determined by re-modulation of these symbols.
   Each firing, one token is produced at the output pin while one token is consumed at the input pin.
2. To control the ISI, the filter takes the first Nyquist criterion as the basis, which provides the method to obtain zero or controlled ISI.
   The impulse response of the filter is obtained from its frequency response, which can be derived from the equation

   $$G_T(f) \times Cf \times G_R(f) = X_d(f) \times e^{j2\pi f t_0}$$

   where
   $G_R(f)$
   is the frequency response of this receiving filter
   $G_T(f)$
   is that of the shaping filter, and $C(f)$ represents Channel frequency response, which is set to be 1 for AWGN channel.
   $X_d(f)$
   is the desired frequency response of the cascade of the modulator, channel and demodulator.
   t_0
   is a time delay necessary to ensure the physical realizability of the transmitting and receiving filters.
   According to the first Nyquist criterion, $X_d(f)$ should be a raised-cosine function so that the zero ISI is obtained at the sampling instances. The roll-off factor of the raised-cosine function is set to 0.35.
   The following figure illustrates how the impulse response of the receiving filter is determined. After the filter frequency response is calculated the impulse response is determined. FFT is used to transform data between the time and frequency domain. Generally, longer FFT will result in better filter performance; however, simulation time will be lengthy. The FFT length is set to 2^{15} for precision and speed.



$g_R(t)$ Computation

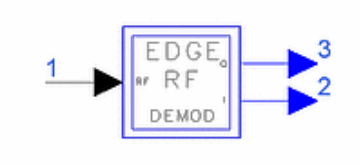
References

1. J. G. Proakis, Digital Communications, Third Edition, McGraw-Hill, Inc., p 557
2. Zhigang, Q. Yasheng, Theories of Modern Communications, (in Chinese), Publishing House of TsingHua University, pp 215-219.

RF Subsystems for EDGE Design Library

- *EDGE RF Demod* (edge)
- *EDGE RF Mod* (edge)
- *EDGE RF RX IFout* (edge)
- *EDGE RF TX IFin* (edge)

EDGE_RF_Demod



Description RF Demodulator
Library EDGE, RF Subsystems
Class TSDFEDGE_RF_Demod

Parameters

Name	Description	Default	Unit	Type	Range
FCarrier	carrier frequency	1.9e9	Hz	real	(0, ∞)
Phase	demodulator reference phase in degrees	0.0	deg	real	(-∞, ∞)
VRef	reference voltage for output calibration	1.0	V	real	(0, ∞)
RIn	input resistance	DefaultRIn	Ohm	real	(0, ∞)

Pin Inputs

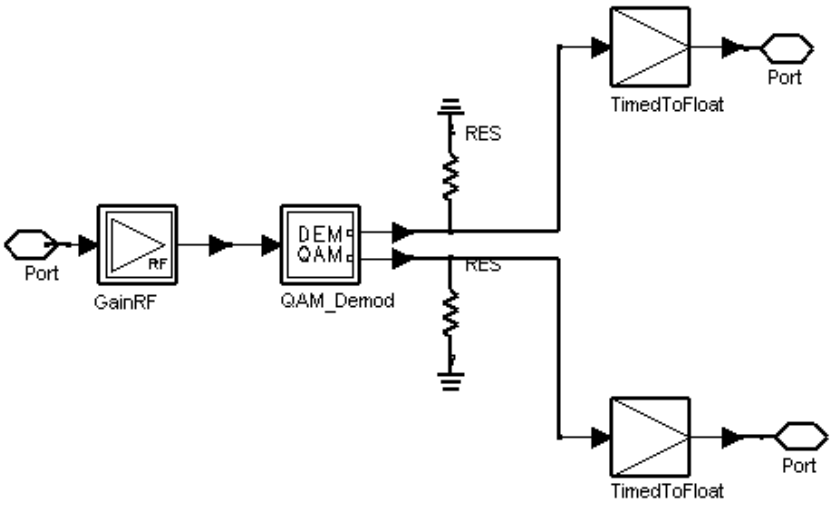
Pin	Name	Description	Signal Type
1	RF_in	RF input	timed

Pin Outputs

Pin	Name	Description	Signal Type
2	I_out	baseband inphase output	real
3	Q_out	baseband quadrature phase output	real

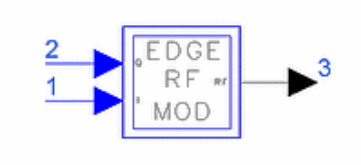
Notes/Equations

1. This is a subnetwork composed of other components. The schematic is shown in the following figure. The input to the demodulator is an RF signal. The output signals are the baseband I and Q components of the input RF signal. For each input sample consumed, one output sample is produced.
2. The EDGE_RF_Demod is calibrated so that its output I and Q waveforms are the same as the I and Q waveforms at the input of the EDGE_RF_Mod when the two components are connected back-to-back. Power at the input of the demodulator is 10 mW = 10 dBm and VRef is set to the same value for both the modulator and demodulator. If the demodulator input power is different from 10 mW, then its VRef parameter should be set appropriately to compensate for that. Let R equal the ratio of 10 mW to the actual input power of the demodulator. Then, the demodulator's VRef should be set to the VRef value of the modulator multiplied by sqrt(R). For example, let's assume that the demodulator input power is 40 mW and the VRef parameter of the modulator is 2. Then, the demodulator VRef must be set to 2 × sqrt(10 / 40) = 2 × (1/2) = 1.



EDGE_RF_Demod Schematic

EDGE_RF_Mod



Description RF Modulator
Library EDGE, RF Subsystems
Class TSDFEDGE_RF_Mod

Parameters

Name	Description	Default	Sym	Unit	Type	Range
FCarrier	carrier frequency	1.9e9	f_c	Hz	real	(0, ∞)
Power	RF output power	0.01	P	W	real	[0, ∞)
VRef	reference voltage for output power calibration	1.0		V	real	(0, ∞)
I_OriginOffset	I origin offset in percent with respect to output rms value	0.0			real	(-∞, ∞)
Q_OriginOffset	Q origin offset in percent with respect to output rms value	0.0			real	(-∞, ∞)
IQ_Rotation	IQ_Rotation in degrees	0.0			real	(-∞, ∞)
FrequencyError	frequency error	0.0	Δ f	Hz	real	(-∞, ∞)
GainImbalance	gain imbalance in dB; Q channel has the gain imbalance applied to it	0.0			real	(-∞, ∞)
PhaseImbalance	phase imbalance in degrees; Q channel has the phase imbalance applied to it	0.0			real	(-∞, ∞)
NDensity	additive noise density in dBm per Hz	-173.975			real	(-∞, ∞)
ROut	output resistance	DefaultROut		Ohm	real	(0, ∞)
TStep	time step	0.0		sec	real	(0, ∞)
PhasePolarity	if set to Invert, Q channel signal is inverted: Normal, Invert	Normal			enum	

Pin Inputs

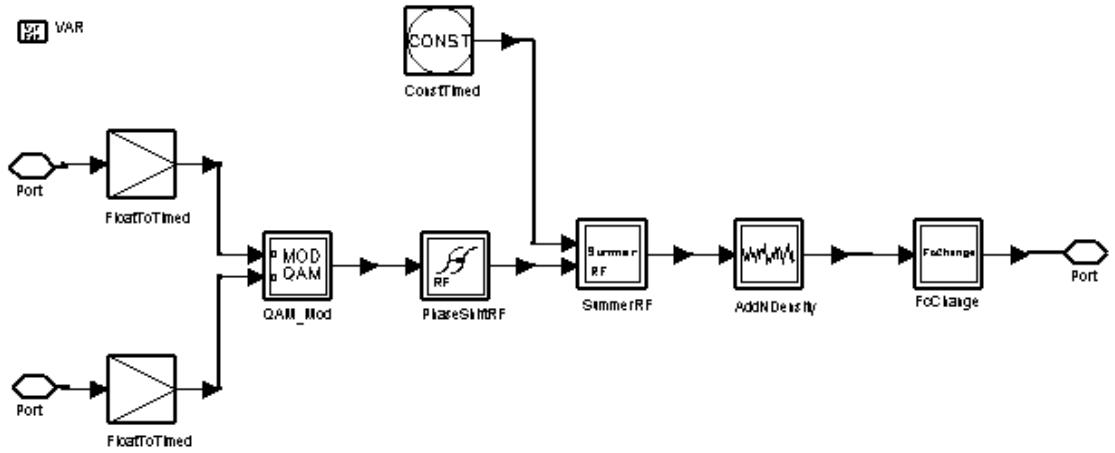
Pin	Name	Description	Signal Type
1	I_in	Baseband inphase input	real
2	Q_in	Baseband quadrature phase input	real

Pin Outputs

Pin	Name	Description	Signal Type
3	RF_out	RF output	timed

Notes/Equations

1. This is a subnetwork composed of other components. The schematic is shown in the following figure. Inputs are the I and Q waveforms of an EDGE baseband signal. The input signals are used to modulate the in-phase and quadrature-phase carriers of a QAM modulator. For each input sample consumed, one output sample is produced.



EDGE_RF_Mod Schematic

2. The VRef parameter is used to calibrate the modulator. Vref is the input voltage value that results in an instantaneous output power on a matched load equal to P. In order to get an average output power on a matched load equal to P, the input rms voltage must equal VRef. Thus, in order to calibrate the modulator, VRef must be set to the input rms voltage.
   If the input signal is a framed EDGE signal with different power levels during each time slot, then the output power levels during each time slot will be proportional to the input power levels during the same time slot. For example, assume Power is set to 13 dBm = 20 mW, VRef is set to 1, and the input signal has an rms voltage of 1 during the first time slot, an rms voltage of 2 during the second time slot, and an rms voltage of 1/sqrt(2) during the third time slot.
   Then, average output power during the first time slot will be 13 dBm = 20 mW, during the second time slot it will be 19 dBm = 80 mW ($=20 \times (2 / VRef)^2$), and during the third time slot it will be 10 dBm = 10 mW ($=20 \times (sqrt(2) / VRef)^2$).
3. The PhasePolarity parameter can be used to invert the polarity of the Q channel signal before modulation. Depending on the configuration and number of mixers in the transmitter and receiver, the output of the demodulator may be inverted. If such a configuration is used, the Q channel signal can be correctly recovered by setting this parameter to Invert.
4. The I_OriginOffset, Q_OriginOffset, IQ_Rotation, FrequencyError, GainImbalance, PhaseImbalance and NDensity parameters are used to add certain impairments to the ideal transmitted signal. The impairments are added in the order described here. The I and Q baseband input signals are applied to the I and Q inputs of a QAM

modulator, which will apply the gain and phase imbalance to its quadrature phase input. The QAM modulator will also introduce the FrequencyError. The signal at the output of the QAM modulator is given by

$$V_3(t) = A\left(V_1(t)\cos(\omega_c t) - gV_2(t)\sin\left(\omega_c t + \frac{\phi\pi}{180}\right)\right)$$

where A is a scaling factor that depends on the Power, VRef and ROut parameters specified by the designer, V_1 (t) is the in-phase input, V_2 (t) is the quadrature phase input $\omega_c = 2\pi(f_c + \Delta f)$, g is the gain imbalance ($g=10^{GainImbalance / 20}$), and φ (in degrees) is the phase imbalance.
Next, the signal V_3 (t) is rotated by IQ_Rotation degrees. Then, the I_OriginOffset and Q_OriginOffset are applied to the rotated signal. Note that the amounts specified are percentages with respect to the output rms voltage. The output rms voltage is given by $\sqrt{2 \cdot ROut \cdot P}$. Finally, additive noise of spectral density NDensity dBm/Hz is added to the signal.
To generate an ideal signal I_OriginOffset, Q_OriginOffset, IQ_Rotation, FrequencyError, GainImbalance and PhaseImbalance must all be set to zero, with NDensity set to a very small value (the value of −228.59925 dBm/Hz corresponds to a resistor temperature of 0.001 Kelvin).
Note that the characterization frequency for the signal at the output of this component is always f_c, no matter what the value of Δf is.

5. The Power parameter is used to set the modulator's output RF power. This is true for an ideal transmitted signal (no impairments added) or when small impairments are added. If large impairments are added to the signal, especially by using the GainImbalance, I_OriginOffset and Q_OriginOffset parameters, then the output RF power may be different from the value of the Power parameter.

EDGE_RF_RX_IFout

Description RF receiver with RF input and IF output
Library EDGE, RF Subsystems
Class TSDFEDGE_RF_RX_IFout

Parameters

Name	Description	Default	Unit	Type	Range
RX_AntTemp	receiving antenna noise temperature, in degrees Kelvin	150		real	(0, ∞)
RX_Gain	receiver gain, in dB	50 dB		real	(-∞, ∞)
RX_NF	receiver noise figure	5 dB		real	(0, ∞)
RF_Freq	input RF frequency	900e6 Hz	Hz	real	(0, ∞)
RF_BW	RF filter bandwidth	25e6 Hz	Hz	real	(0, ∞)
IF_Freq1	1st IF frequency	100e6 Hz	Hz	real	(0, ∞)
IF_Freq2	2nd IF frequency	400e3 Hz	Hz	real	(0, ∞)
IF_BW	IF filter bandwidth	30e3 Hz	Hz	real	(0, ∞)
IP3in	3rd order intercept point at input, in dBm	dbmtow(-25)	W	real	(-∞, ∞
RIn	input resistance	DefaultRIn	Ohm	real	(0, ∞)
ROut	output resistance	DefaultROut	Ohm	real	(0, ∞)

Pin Inputs

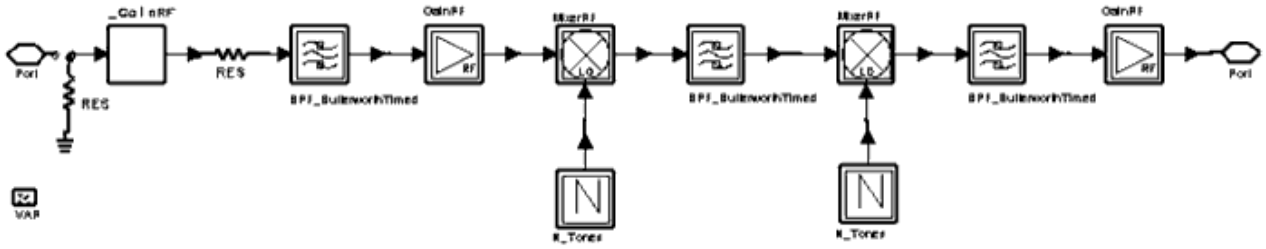
Pin	Name	Description	Signal Type
1	input	input RF signal	timed

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output IF signal	timed

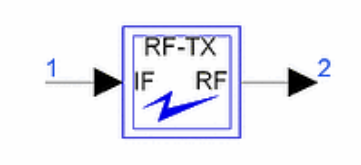
Notes/Equations

1. This is a subnetwork composed of other components. The schematic is shown in the following figure. The receiver is used to convert input RF signal to output IF signal with nonlinear distortion and additive noise.
2. RX_Gain and IP3in parameters determine the nonlinear distortion. RX_AntTemp and RX_NF parameters determine the additive noise.
3. This component uses the double down-conversion (super-heterodyne) scheme. Low-side LO signals are used. Consequently there is no spectral inversion at the output.
4. If RF_BW is much greater than IF_BW, and the simulation time step is set according to IF_BW, a warning message from the RF filter may be issued. This is because RF filter bandwidth is not fully characterized. This usually does not affect the simulation accuracy.
5. The output signal-noise ratio is determined as follows: S/N (in dB) = S − N, S = P_in + RX_Gain, N = N0_output × IF_BW, N0_output = N0_input × RX_Gain + RX_NF, N0_input = K × RX_AntTemp, where K is Boltzmann's constant.



EDGE_RF_RX_IFout Schematic

EDGE_RF_TX_IFin



Description RF transmitter with IF input and RF output
Library EDGE, RF Subsystems
Class TSDFEDGE_RF_TX_IFin

Parameters

Name	Description	Default	Unit	Type	Range
IF_Freq	input IF frequency	400e3 Hz	Hz	real	(0, ∞)
RF_Freq	output RF frequency	900e6 Hz	Hz	real	(0, ∞)
TX_Gain	transmitter gain in dB	80 dB		real	(-∞, ∞)
PSat	saturated output power	dbmtow(35)	W	real	(-∞, ∞)
RIn	input resistance	DefaultRIn	Ohm	real	(0, ∞)
ROut	output resistance	DefaultROut	Ohm	real	(0, ∞)
RTemp	resistor physical temperature, C	DefaultRTemp		real	(-∞, ∞)
TStep	time step	0.0	sec	real	(0, ∞)
SAW_Aripple	amplitude ripple of SAW filter	1.0		real	[0, ∞)

Pin Inputs

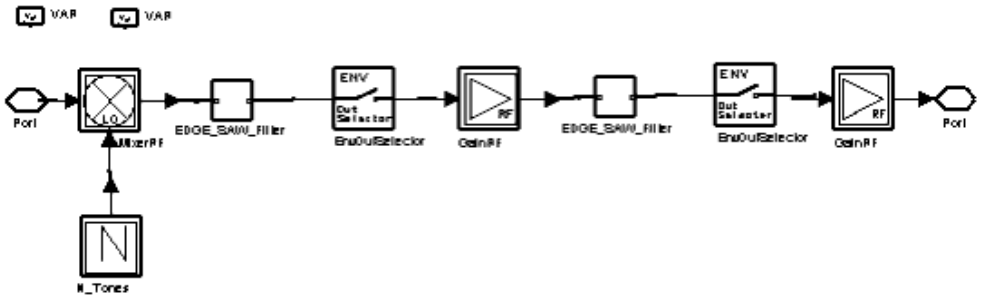
Pin	Name	Description	Signal Type
1	input	input IF signal	timed

Pin Outputs

Pin	Name	Description	Signal Type
2	output	output RF signal	timed

Notes/Equations

1. This is a subnetwork composed of other components. The schematic is shown in the following figure. The transmitter is used to convert input IF signal to output RF signal with nonlinear distortion and additive noise.
2. Nonlinear distortion is determined by PSat parameter. PSat parameter models am-am distortion only. (It does not model am-pm distortion; the GComp parameter on TxPowerAmp is recommended for this.)

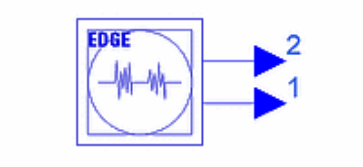


EDGE_RF_TX_IFin Schematic

Signal Sources for EDGE Design Library

- *EDGE ActiveIdleSrc* (edge)
- *EDGE BTS MCS5 PwrCtrlSrc* (edge)
- *EDGE BTS MCS6 PwrCtrlSrc* (edge)
- *EDGE BTS MCS7 PwrCtrlSrc* (edge)
- *EDGE BTS MCS8 PwrCtrlSrc* (edge)
- *EDGE BTS MCS9 PwrCtrlSrc* (edge)
- *EDGE DataPattern* (edge)
- *EDGE FramedSrc* (edge)
- *EDGE MS MCS5 PwrCtrlSrc* (edge)
- *EDGE MS MCS6 PwrCtrlSrc* (edge)
- *EDGE MS MCS7 PwrCtrlSrc* (edge)
- *EDGE MS MCS8 PwrCtrlSrc* (edge)
- *EDGE MS MCS9 PwrCtrlSrc* (edge)
- *EDGE PatternedSrc* (edge)
- *EDGE RandomSrc* (edge)
- *EDGE Signal Source* (edge)
- *EDGE Source* (edge)

EDGE_ActiveIdleSrc



Description EDGE signal source with active and idle time slots
Library EDGE, Signal Sources
Class SDFEDGE_ActiveIdleSrc

Parameters

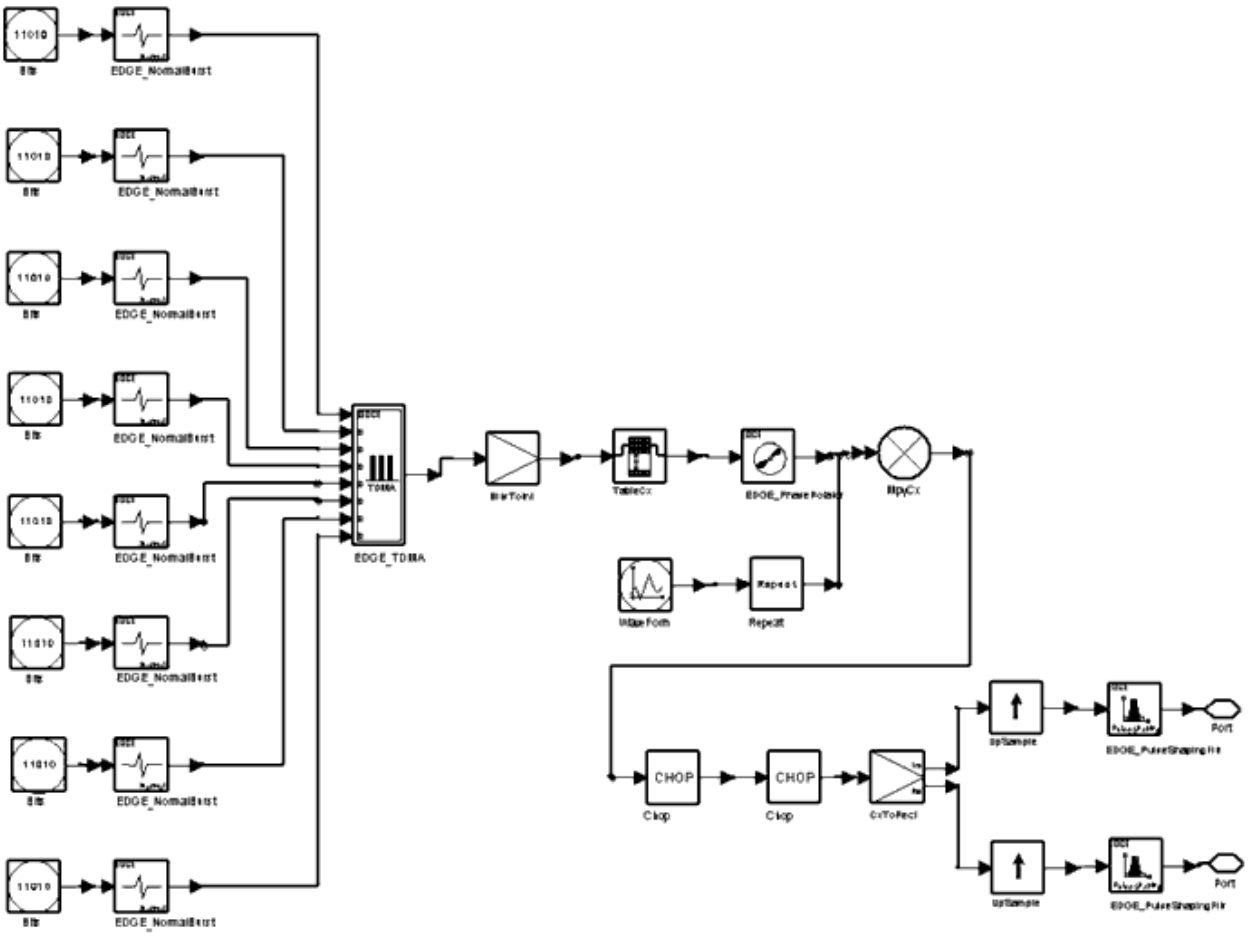
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_State	state of each time slot: 0 for idle, 1 for active	0 0 0 0 0 0 0 0	int array	

Pin Outputs

Pin	Name	Description	Signal Type
1	output_I	inphase output	real
2	output_Q	quadrature output	real

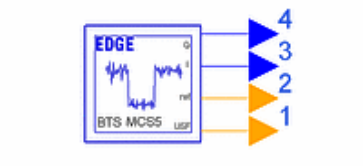
Notes/Equations

1. This subnetwork is used to generate the framed and modulated EDGE signal.
2. The schematic for this subnetwork is shown in the following diagram. Eight random bit source components are used to simulate the data of eight users. A normal burst for each user is constructed by adding the training sequence, tail bits, guard bits, and stealing flag bits to the user data.
3. Data of each burst is 8PSK modulated. TS_State controls the output signal power of each time slot. For example, if TS_State = "0 1 0 0 0 0 0 0" , only symbols in the second time slot are transmitted and the transmitted power of the other seven time slots is 0.



EDGE_ActiveIdleSrc Schematic

EDGE_BTS_MCS5_PwrCtrlSrc



Description EDGE signal source for reference sensitivity level test
Library EDGE, Signal Sources
Class SDFEDGE_BTS_MCS5_PwrCtrlSrc

Parameters

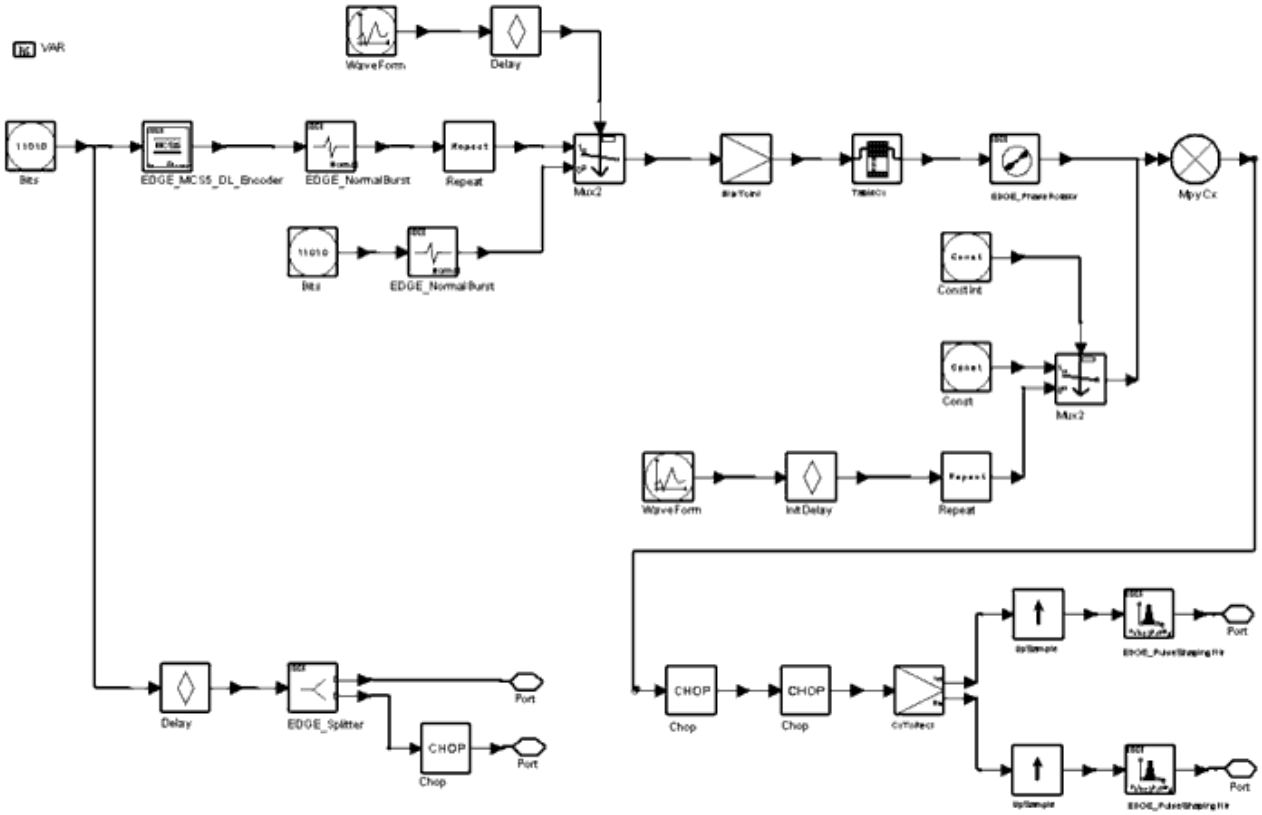
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_Measured	time slot measured	0	int	[0, 7]
TSC	training sequence code	0	int	[0, 7]
PwrState	power control pattern: Power controlled, Full power in each time slot	Power controlled	enum	
dB_NAllocGain	gain of slots not allocated to MS, in dB	0	real	(-∞, ∞)

Pin Outputs

Pin	Name	Description	Signal Type
1	USF_ref	reference output of USF delay adjusted	int
2	ref	reference output of bit source with delay adjusted	int
3	I	inphase output	real
4	Q	quadrature output	real

Notes/Equations

1. This subnetwork is used to generate the encoded, framed, modulated and power-controlled downlink EDGE signal for PDTCH/MCS-5.
2. The schematic for this subnetwork is shown in the following diagram. A random bit source component is used to simulate the transmitted RLC blocks of the used time slot, and the bit stream is encoded with EDGE_MCS5_DL_Encoder, then a normal burst is constructed with EDGE_NormalBurst. Another random bit source is used to simulate the data of the other seven unused time slots. And a frame is constructed with a Mux2 component. The framed data is modulated and power-controlled with a MpyCx component.
3. The random bit source to simulate the data of the used time slot is delayed two RLC blocks before output because of the delay of the decoder in the receiver. Only the USF bits and data bits is output, the header bits is deleted.



EDGE_BTS_MCS5_PwrCtrlSrc Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BTS_MCS6_PwrCtrlSrc

Description EDGE signal source for reference sensitivity level test
Library EDGE, Signal Sources
Class SDFEDGE_BTS_MCS6_PwrCtrlSrc

Parameters

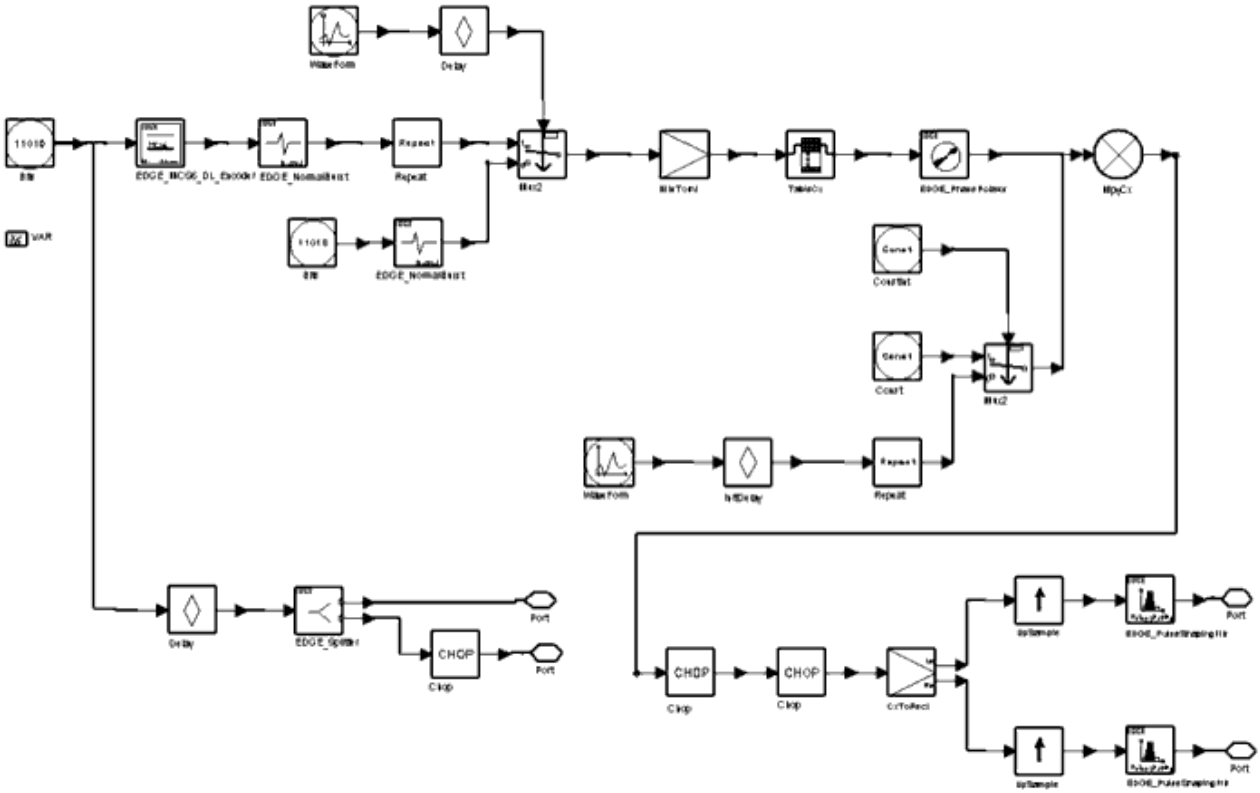
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_Measured	time slot measured	0	int	[0, 7]
TSC	training sequence code	0	int	[0, 7]
PwrState	power control pattern: Power controlled, Full power in each time slot	Power controlled	enum	
dB_NAllocGain	gain of slots not allocated to MS, in dB	0	real	(-∞, ∞)

Pin Outputs

Pin	Name	Description	Signal Type
1	USF_ref	reference output of USF delay adjusted	int
2	ref	reference output of bit source with delay adjusted	int
3	I	inphase output	real
4	Q	quadrature output	real

Notes/Equations

1. This subnetwork is used to generate the encoded, framed, modulated and power-controlled downlink EDGE signal for PDTCH/MCS-6.
2. The schematic for this subnetwork is shown in the following figure. A random bit source component is used to simulate the transmitted RLC blocks of the used time slot, and the bit stream is encoded with EDGE_MCS6_DL_Encoder, then a normal burst is constructed with EDGE_NormalBurst. Another random bit source is used to simulate the data of the other seven unused time slots. And a frame is constructed with a Mux2 component. The framed data is modulated and power-controlled with a MpyCx component.
3. The random bit source to simulate the data of the used time slot is delayed two RLC blocks before output because of the delay of the decoder in the receiver. Only the USF bits and data bits is output, the header bits is deleted.



EDGE_BTS_MCS6_PwrCtrlSrc Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BTS_MCS7_PwrCtrlSrc

Description EDGE signal source for reference sensitivity level test
Library EDGE, Signal Sources
Class SDFEDGE_BTS_MCS7_PwrCtrlSrc

Parameters

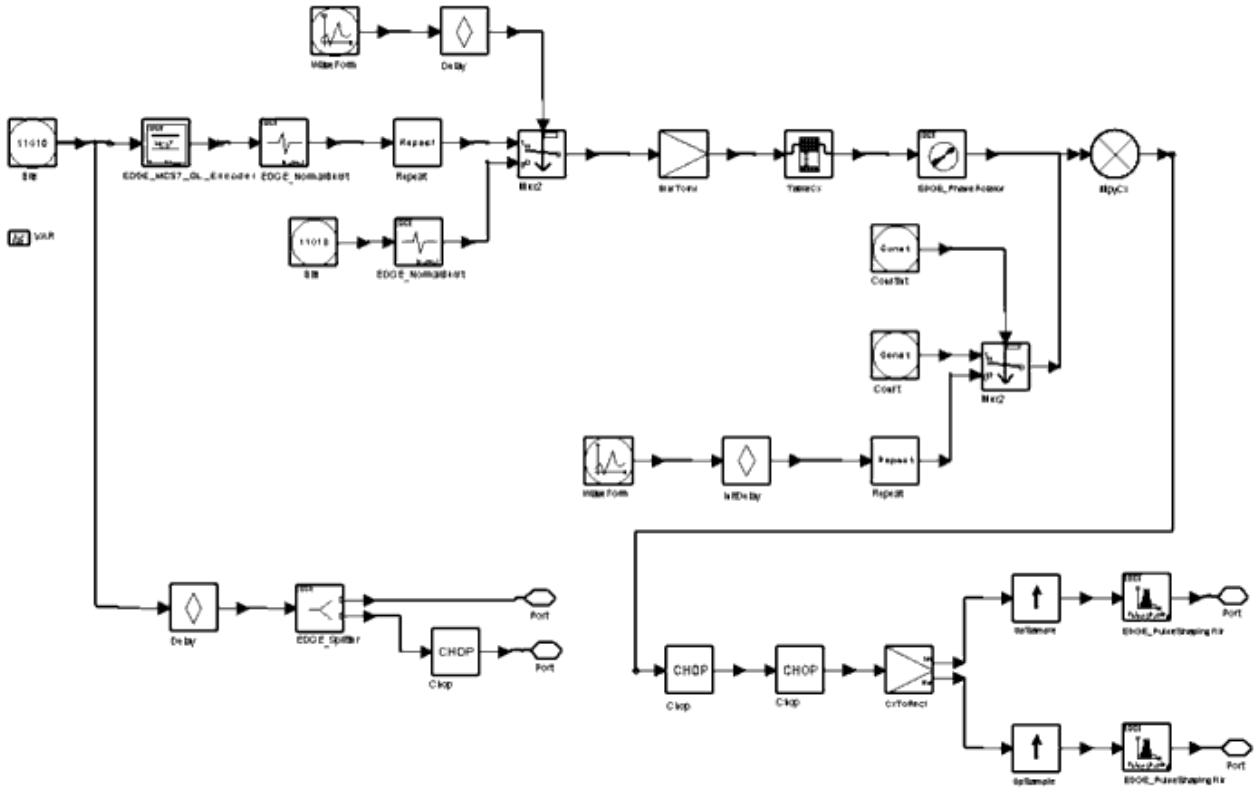
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_Measured	time slot measured	0	int	[0, 7]
TSC	training sequence code	0	int	[0, 7]
PwrState	power control pattern: Power controlled, Full power in each time slot	Power controlled	enum	
dB_NAllocGain	gain of slots not allocated to MS, in dB	0	real	(-∞, ∞)

Pin Outputs

Pin	Name	Description	Signal Type
1	USF_ref	reference output of USF delay adjusted	int
2	ref	reference output of bit source with delay adjusted	int
3	I	inphase output	real
4	Q	quadrature output	real

Notes/Equations

1. This subnetwork is used to generate the encoded, framed, modulated and power-controlled downlink EDGE signal for PDTCH/MCS-7.
2. The schematic for this subnetwork is shown in the following figure. A random bit source component is used to simulate the transmitted RLC blocks of the used time slot, and the bit stream is encoded with EDGE_MCS7_DL_Encoder, then a normal burst is constructed with EDGE_NormalBurst. Another random bit source is used to simulate the data of the other seven unused time slots. And a frame is constructed with a Mux2 component. The framed data is modulated and power-controlled with a MpyCx component.
3. The random bit source to simulate the data of the used time slot is delayed one RLC blocks before output because of the delay of the decoder in the receiver. Only the USF bits and data bits is output, the header bits is deleted.

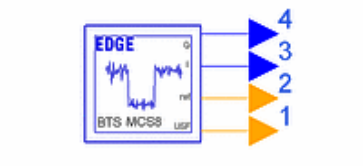


EDGE_BTS_MCS7_PwrCtrlSrc Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BTS_MCS8_PwrCtrlSrc



Description EDGE signal source for reference sensitivity level test
Library EDGE, Signal Sources
Class SDFEDGE_BTS_MCS8_PwrCtrlSrc

Parameters

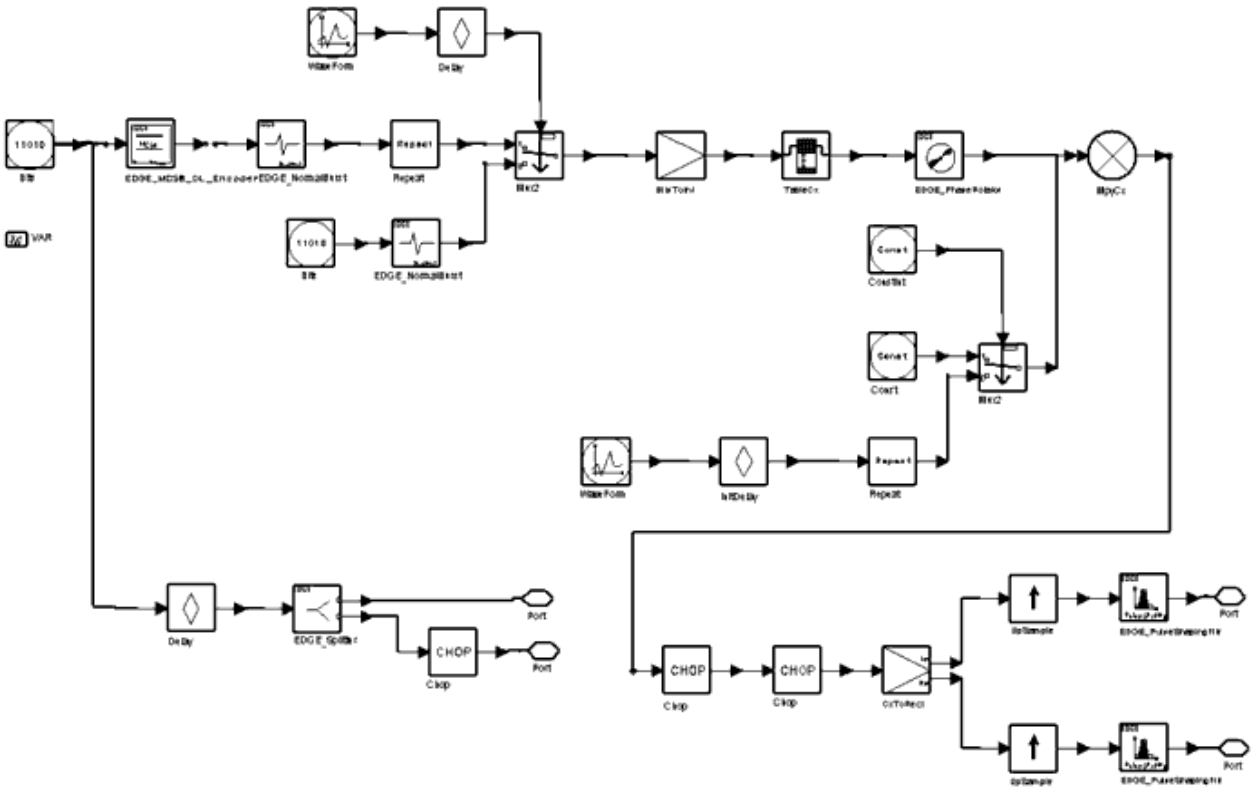
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_Measured	time slot measured	0	int	[0, 7]
TSC	training sequence code	0	int	[0, 7]
PwrState	power control pattern: Power controlled, Full power in each time slot	Power controlled	enum	
dB_NAllocGain	gain of slots not allocated to MS, in dB	0	real	(-∞, ∞)

Pin Outputs

Pin	Name	Description	Signal Type
1	USF_ref	reference output of USF delay adjusted	int
2	ref	reference output of bit source with delay adjusted	int
3	I	inphase output	real
4	Q	quadrature output	real

Notes/Equations

1. This subnetwork is used to generate the encoded, framed, modulated and power-controlled downlink EDGE signal for PDTCH/MCS-8.
2. The schematic for this subnetwork is shown in the following figure. A random bit source component is used to simulate the transmitted RLC blocks of the used time slot, and the bit stream is encoded with EDGE_MCS8_DL_Encoder, then a normal burst is constructed with EDGE_NormalBurst. Another random bit source is used to simulate the data of the other seven unused time slots. And a frame is constructed with a Mux2 component. The framed data is modulated and power-controlled with a MpyCx component.
3. The random bit source to simulate the data of the used time slot is delayed one RLC blocks before output because of the delay of the decoder in the receiver. Only the USF bits and data bits is output, the header bits is deleted.



EDGE_BTS_MCS8_PwrCtrlSrc Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_BTS_MCS9_PwrCtrlSrc

Description EDGE signal source for reference sensitivity level test
Library EDGE, Signal Sources
Class SDFEDGE_BTS_MCS9_PwrCtrlSrc

Parameters

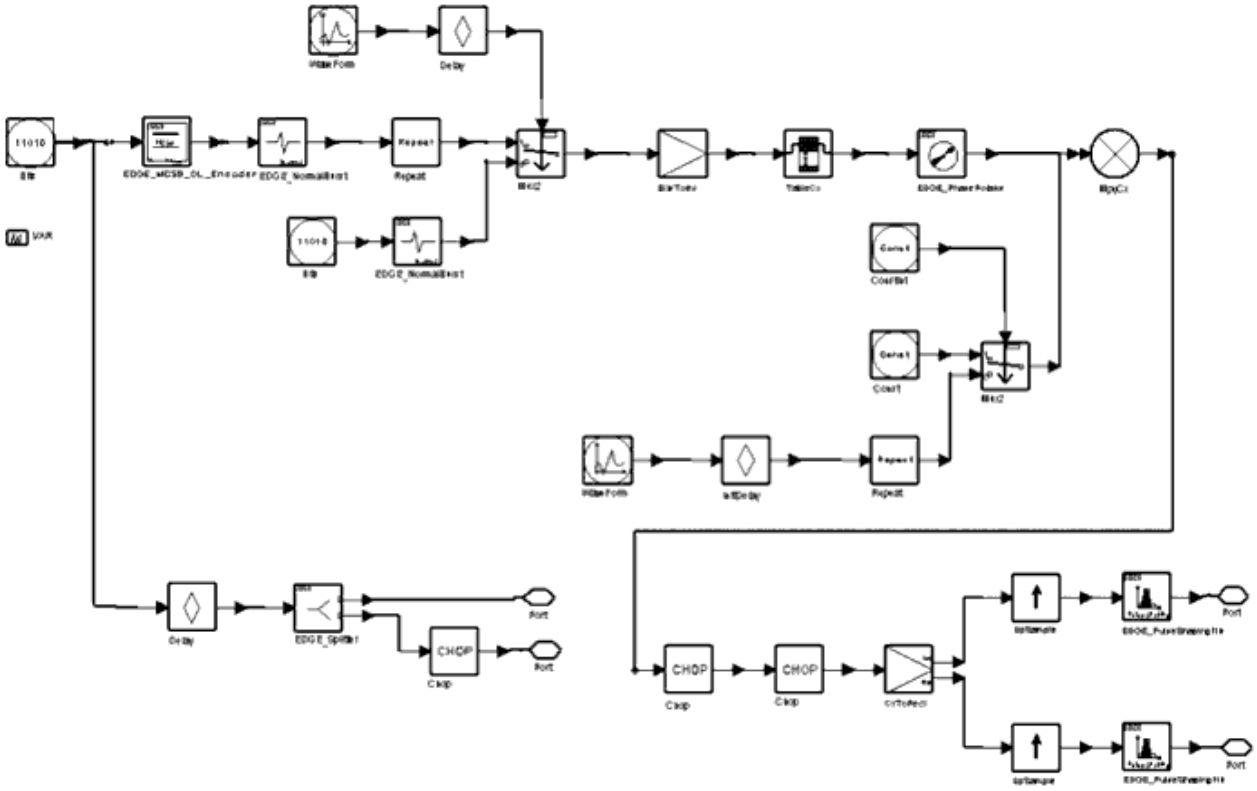
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_Measured	time slot measured	0	int	[0, 7]
TSC	training sequence code	0	int	[0, 7]
PwrState	power control pattern: Power controlled, Full power in each time slot	Power controlled	enum	
dB_NAllocGain	gain of slots not allocated to MS, in dB	0	real	(-∞, ∞)

Pin Outputs

Pin	Name	Description	Signal Type
1	USF_ref	reference output of USF delay adjusted	int
2	ref	reference output of bit source with delay adjusted	int
3	I	inphase output	real
4	Q	quadrature output	real

Notes/Equations

1. This subnetwork is used to generate the encoded, framed, modulated and power-controlled downlink EDGE signal for PDTCH/MCS-9.
2. The schematic for this subnetwork is shown in the following figure. A random bit source component is used to simulate the transmitted RLC blocks of the used time slot, and the bit stream is encoded with EDGE_MCS9_DL_Encoder, then a normal burst is constructed with EDGE_NormalBurst. Another random bit source is used to simulate the data of the other seven unused time slots. And a frame is constructed with a Mux2 component. The framed data is modulated and power-controlled with a MpyCx component.
3. The random bit source to simulate the data of the used time slot is delayed one RLC blocks before output because of the delay of the decoder in the receiver. Only the USF bits and data bits is output, the header bits is deleted.

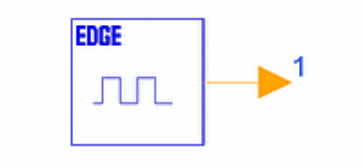


EDGE_BTS_MCS9_PwrCtrlSrc Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_DataPattern



Description Patterned data source for EDGE
Library EDGE, Signal Sources
Class SDFEDGE_DataPattern

Parameters

Name	Description	Default	Type
DataPattern	data pattern: PN9, PN15, FIX4, _4_1_4_0, _8_1_8_0, _16_1_16_0, _32_1_32_0, _64_1_64_0	PN9	enum

Pin Outputs

Pin	Name	Description	Signal Type
1	output	patterned data output	int

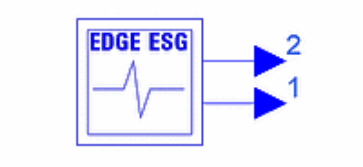
Notes/Equations

1. This model is used to generate one of eight patterned bit streams.
2. For the DataPattern parameter:
   - if PN9 is selected, a 511-bit pseudo-random test pattern is generated according to CCITT RecommendationO.153
   - if PN15 is selected, a 32767-bit pseudo-random test pattern is generated according to CCITT Recommendation O.151
   - if FIX4 is selected, a zero-stream is generated
   - if x_1_x_0 is selected, where x equals 4, 8, 16, 32, or 64, a periodic bit stream is generated, with the period being 2 × x. In one period, the first x bits are 1s and the second x bits are 0s.

References

1. CCITT, Recommendation O.151(10/92).
2. CCITT, Recommendation O.153(10/92).

EDGE_FramedSrc



Description Framed signal source
Library EDGE, Signal Sources
Class SDFEDGE_FramedSrc

Parameters

Name	Description	Default	Type	Range
BurstSpecVersion	EDGE specification for normal burst; if choose Basic, each burst has 156 symbols, otherwise complys with GSM 8.3.0 Release 1999: Basic, GSM_8_3_0_Release_1999	Basic	enum	
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_State	state of each time slot; 0 for idle, 1 for active	1 1 1 1 1 1 1 1	int array	[0, 1]
TS_Type	type of data in each time slot; 0 for non-framed data,1 for framed data	1 1 1 1 1 1 1 1	int array	[0, 1]
DataPattern0	data pattern of time slot 0: PN9 for time slot0, PN15 for time slot0, FIX4 for time slot0, _4_1_4_0 for time slot0, _8_1_8_0 for time slot0, _16_1_16_0 for time slot0, _32_1_32_0 for time slot0, _64_1_64_0 for time slot0	PN9 for time slot0	enum	
DataPattern1	data pattern of time slot 1: PN9 for time slot1, PN15 for time slot1, FIX4 for time slot1, _4_1_4_0 for time slot1, _8_1_8_0 for time slot1, _16_1_16_0 for time slot1, _32_1_32_0 for time slot1, _64_1_64_0 for time slot1	PN9 for time slot1	enum	
DataPattern2	data pattern of time slot 2: PN9 for time slot2, PN15 for time slot2, FIX4 for time slot2, _4_1_4_0 for time slot2, _8_1_8_0 for time slot2, _16_1_16_0 for time slot2, _32_1_32_0 for time slot2, _64_1_64_0 for time slot2	PN9 for time slot2	enum	
DataPattern3	data pattern of time slot 3: PN9 for time slot3, PN15 for time slot3, FIX4 for time slot3, _4_1_4_0 for time slot3, _8_1_8_0 for time slot3, _16_1_16_0 for time slot3, _32_1_32_0 for time slot3, _64_1_64_0 for time slot3	PN9 for time slot3	enum	
DataPattern4	data pattern of time slot 4: PN9 for time slot4, PN15 for time slot4, FIX4 for time slot4, _4_1_4_0 for time slot4, _8_1_8_0 for time slot4, _16_1_16_0 for time slot4, _32_1_32_0 for time slot4, _64_1_64_0 for time slot4	PN9 for time slot4	enum	
DataPattern5	data pattern of time slot 5: PN9 for time slot5, PN15 for time slot5, FIX4 for time slot5, _4_1_4_0 for time slot5, _8_1_8_0 for time slot5, _16_1_16_0 for time slot5, _32_1_32_0 for time slot5, _64_1_64_0 for time slot5	PN9 for time slot5	enum	
DataPattern6	data pattern of time slot 6: PN9 for time slot6, PN15 for time slot6, FIX4 for time slot6, _4_1_4_0 for time slot6, _8_1_8_0 for time slot6, _16_1_16_0 for time slot6, _32_1_32_0 for time slot6, _64_1_64_0 for time slot6	PN9 for time slot6	enum	
DataPattern7	data pattern of time slot 7: PN9 for time slot7, PN15 for time slot7, FIX4 for time slot7, _4_1_4_0 for time slot7, _8_1_8_0 for time slot7, _16_1_16_0 for time slot7, _32_1_32_0 for time slot7, _64_1_64_0 for time slot7	PN9 for time slot7	enum	
PwrType	power on and power off type: None, Linear, Cosine	None	enum	
RampLength	power on and power off length	4	int	[0, 156]
RampUpScramble	scramble of ramp up function	1 1 1 1	real array	(-∞,∞)
RampDownScramble	scramble of ramp down function	1 1 1 1	real array	(-∞,∞)
Continues	adding ramp between active slots or not: NO, YES	NO	enum	

Pin Inputs

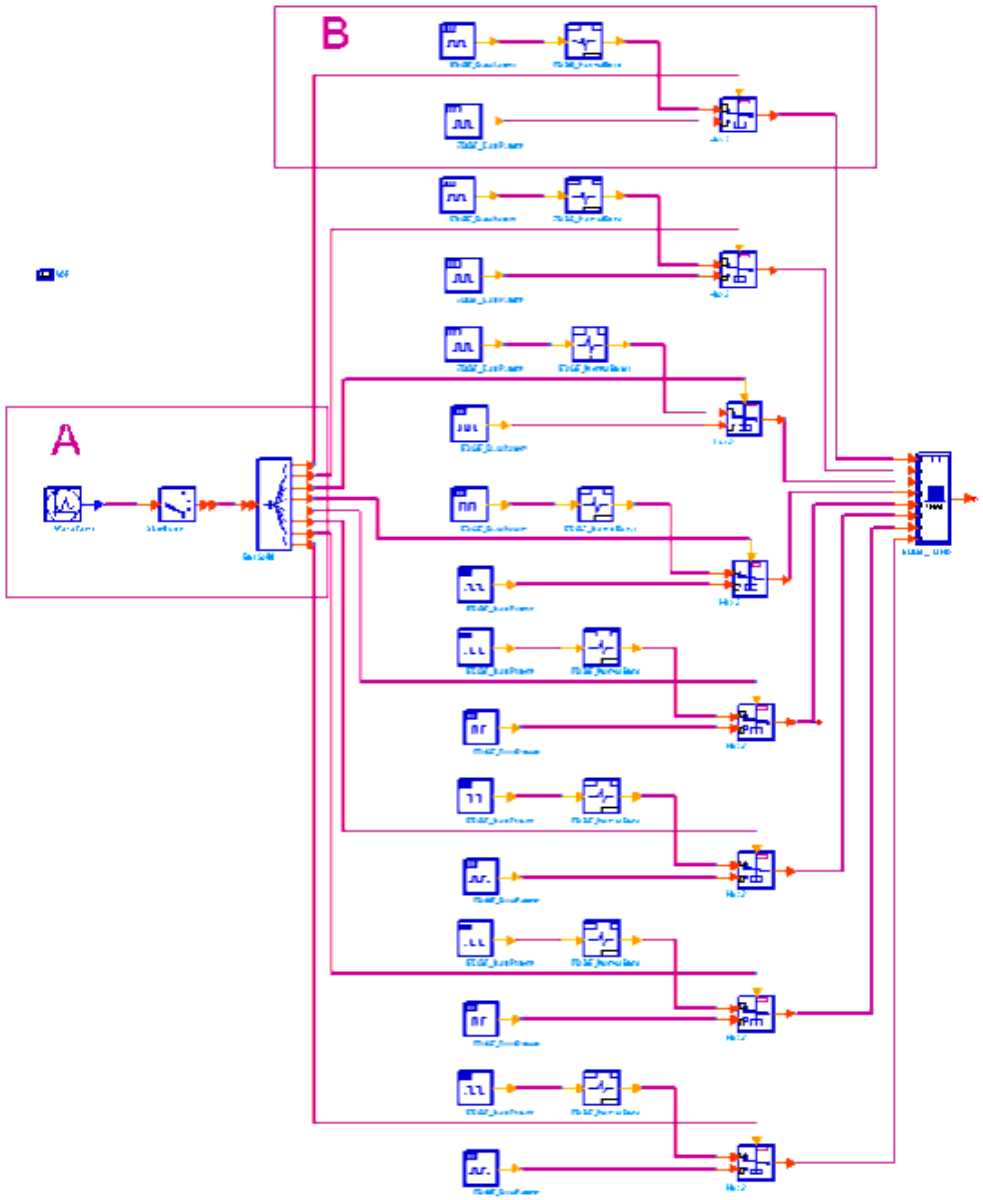
Pin	Name	Description	Signal Type
1	output_I	inphase output	real
2	output_Q	quadrature output	real

Pin Outputs

Pin No.	Name	Descriptions	Signal Type
1	output_I	inphase output	floating-point
2	output_Q	quadrature output	floating-point

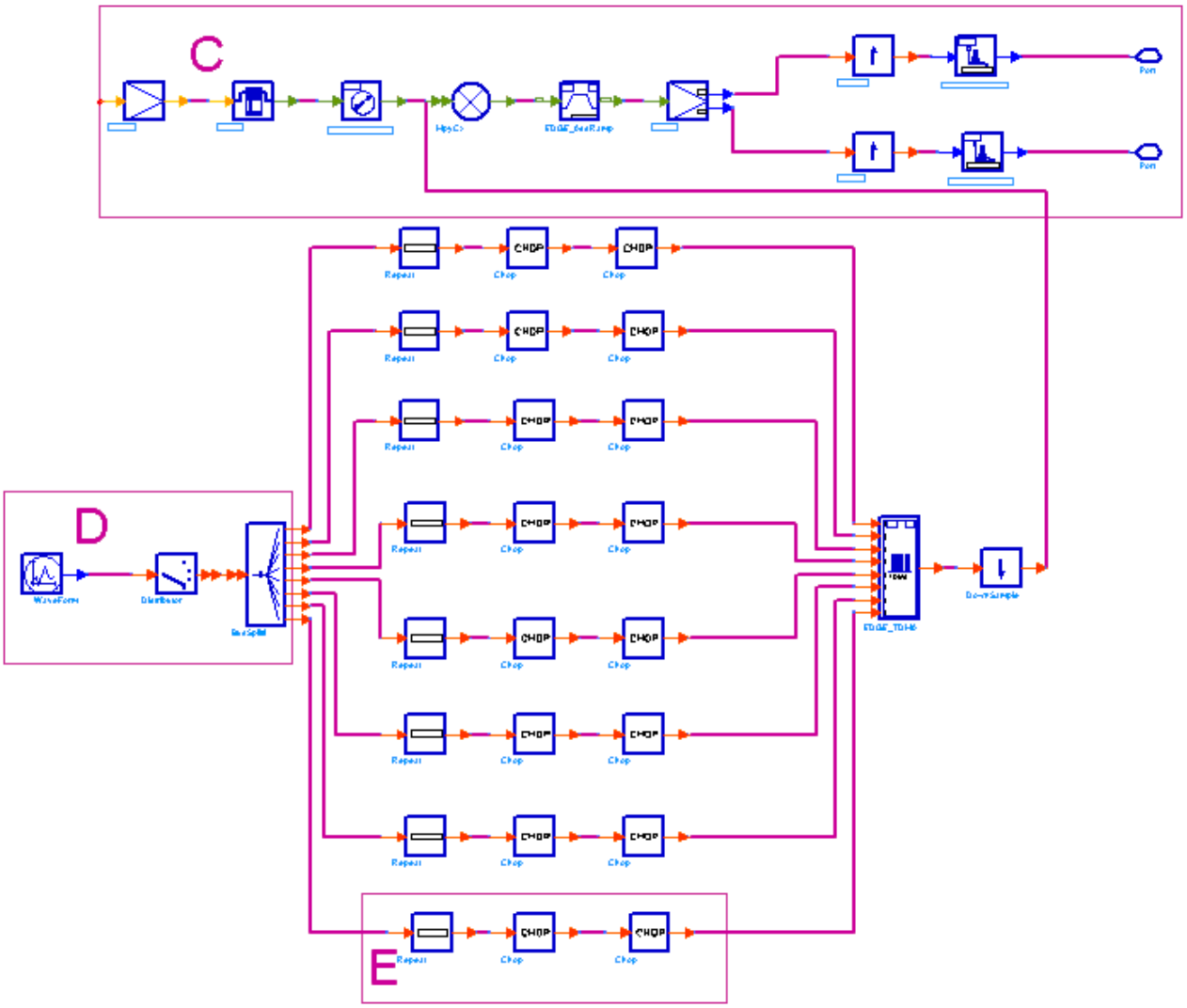
Notes/Equations

1. This subnetwork is used to generate a patterned, framed and modulated EDGE signal. The schematic for this subnetwork is shown in the next two figures.
   In the figure below, components inside dashed frame A generate data of one time slot. Eight such branches simulate the data of eight time slots in one TDMA frame. There are two paths in each branch: the upper path generates data with burst structures, the lower path generates data without burst structures. TS_Type controls whether the exported data of each time slot have burst structures or not, which is implemented by components inside dashed frame B. The data pattern of each time slot can be configured by DataPattern n (n= 0 to 7, which corresponds to eight time slots). EDGE_TDMA combines the data from eight time slots into one TDMA frame.



EDGE_FramedSrc Schematic (1 of 2)

In the figure below, components inside dashed frame C perform mapping 3 bits to 1 symbol, phase-rotating, ramping up and down, up-sampling and pulse-shaping. Components inside dashed frame D and E control whether a time slot is active or idle using the parameter TS_State. If 1 is imported from dashed frame D to E, the modulated data (except guard symbols of this slot) are exported and the guard symbols are set to 0. If 0 is imported, the modulated data including guard symbols are all set to 0. EDGE_TDMA combines the control bits of eight time slots to control the modulated data output of each frame.



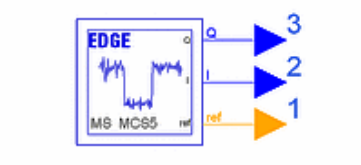
EDGE_FramedSrc Schematic (2 of 2)

2. If BurstSpecVersion is set to *Basic* , each burst in one TDMA frame contains 156 symbols.
   If BurstSpecVersion is set to *GSM_8_3_0_Release_1999* , the first and the fifth bursts in one TDMA frame contain 157 symbols, the other bursts contain 156 symbols (as specified in GSM 05.02, version 8.3.0, Release 1999).

References

1. CCITT, Recommendation O.151(10/92).
2. CCITT, Recommendation O.153(10/92).
3. GSM 05.02, version 8.3.0, Release 1999.
4. GSM 05.05, version 8.3.0, Release 1999.
5. GSM 05.10 for TDMA frame construction

EDGE_MS_MCS5_PwrCtrlSrc



Description EDGE signal source for reference sensitivity level test
Library EDGE, Signal Sources
Class SDFEDGE_MS_MCS5_PwrCtrlSrc

Parameters

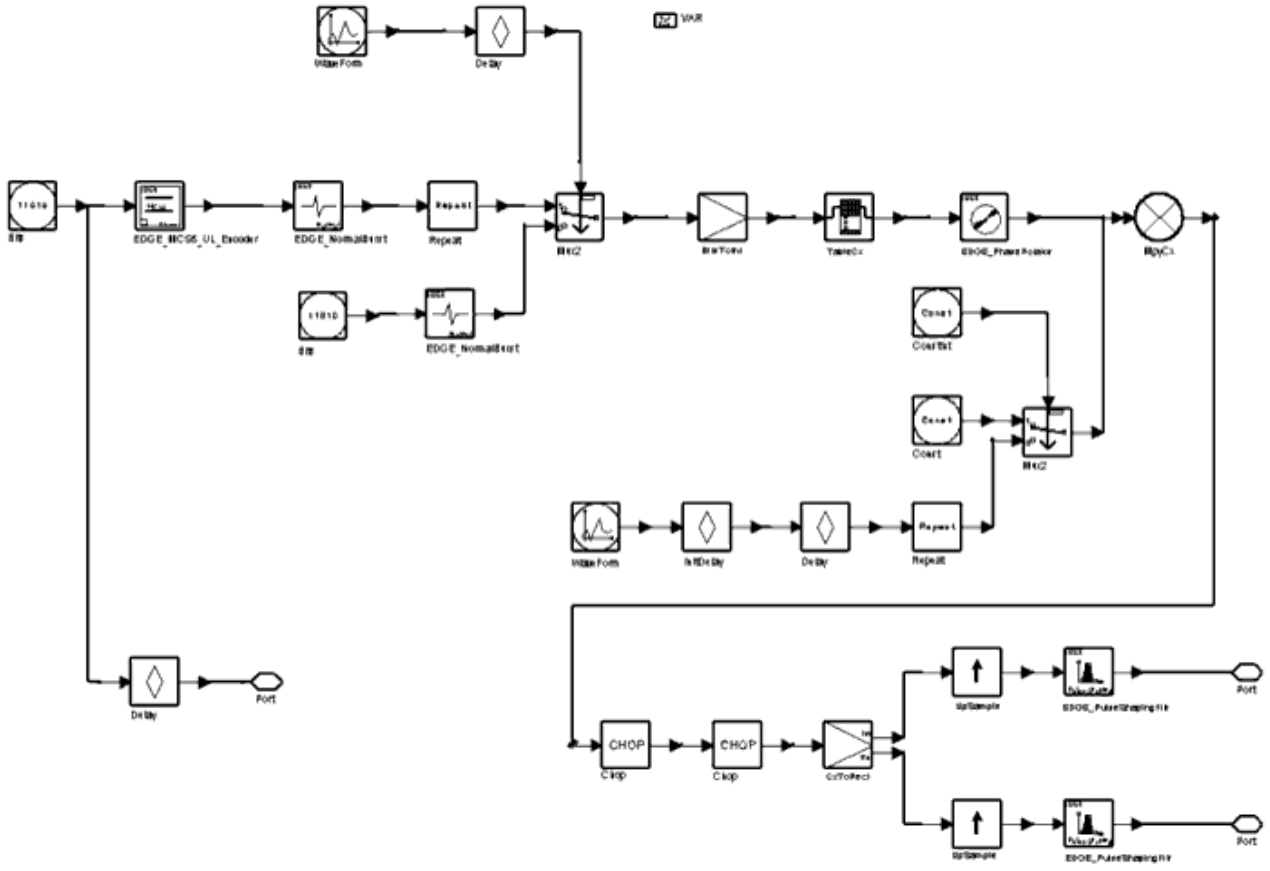
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_Measured	time slot measured	0	int	[0, 7]
TSC	training sequence code	0	int	[0, 7]
PwrState	power control pattern: Power controlled, Full power in each time slot	Power controlled	enum	

Pin Outputs

Pin	Name	Description	Signal Type
1	ref	reference output of bit source with delay adjusted	int
2	I	inphase output	real
3	Q	quadrature output	real

Notes/Equations

1. This subnetwork is used to generate the encoded, framed, modulated and power-controlled downlink EDGE signal for PDTCH/MCS-5.
2. The schematic for this subnetwork is shown in the following figure. A random bit source component is used to simulate the transmitted RLC blocks of the used time slot, and the bit stream is encoded with EDGE_MCS5_UL_Encoder, then a normal burst is constructed with EDGE_NormalBurst. Another random bit source is used to simulate the data of the other seven unused time slots. And, a frame is constructed with a Mux2 component. The framed data is modulated and power-controlled with a MpyCx component.
3. The random bit source to simulate the data of the used time slot is delayed one RLC blocks before output because of the delay of the decoder in the receiver.

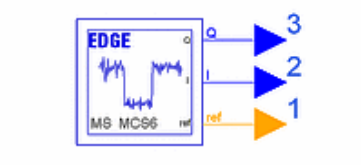


EDGE_MS_MCS5_PwrCtrlSrc Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MS_MCS6_PwrCtrlSrc



Description EDGE signal source for reference sensitivity level test
Library EDGE, Signal Sources
Class SDFEDGE_MS_MCS6_PwrCtrlSrc

Parameters

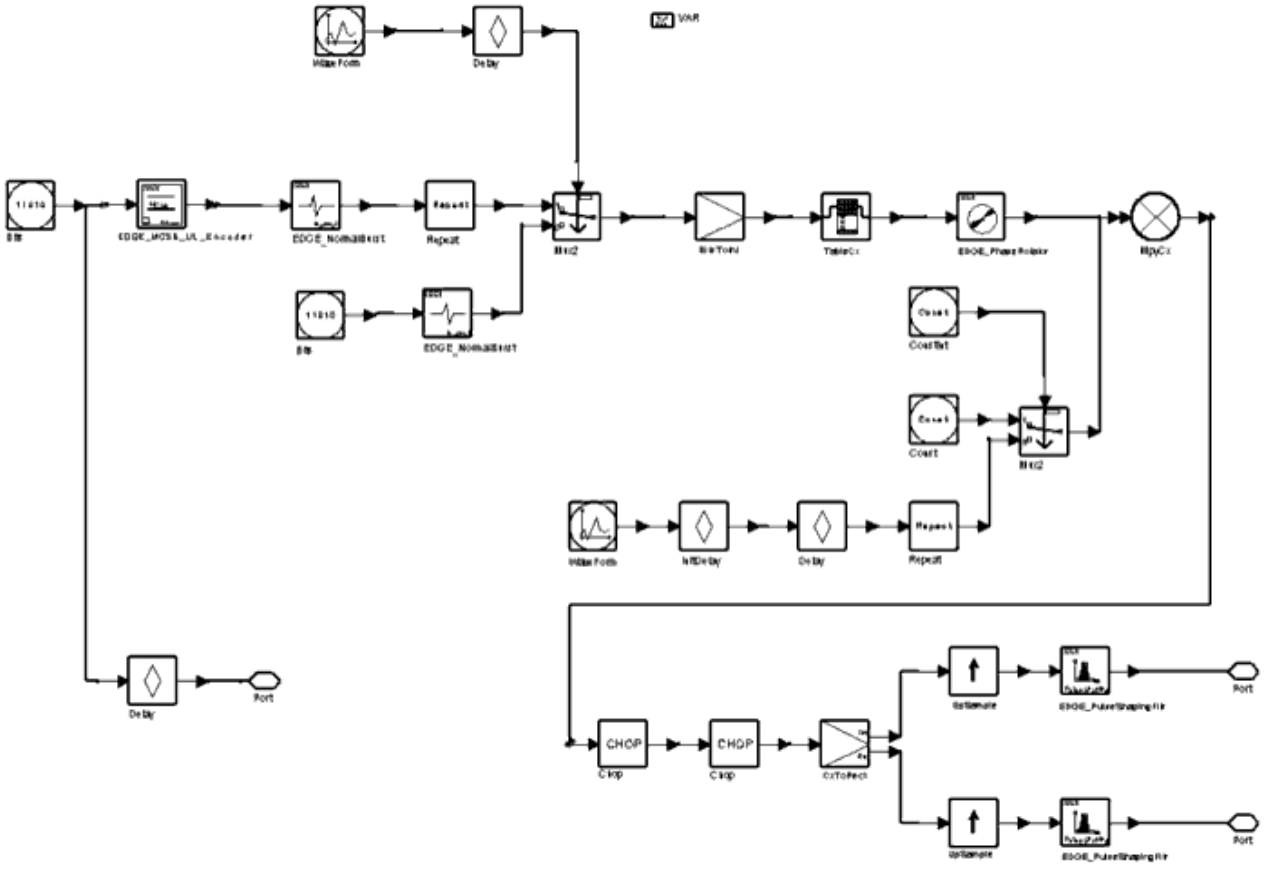
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_Measured	time slot measured	0	int	[0, 7]
TSC	training sequence code	0	int	[0, 7]
PwrState	power control pattern: Power controlled, Full power in each time slot	Power controlled	enum	

Pin Outputs

Pin	Name	Description	Signal Type
1	ref	reference output of bit source with delay adjusted	int
2	I	inphase output	real
3	Q	quadrature output	real

Notes/Equations

1. This subnetwork is used to generate the encoded, framed, modulated and power-controlled downlink EDGE signal for PDTCH/MCS-6.
2. The schematic for this subnetwork is shown in the following figure. A random bit source component is used to simulate the transmitted RLC blocks of the used time slot, and the bit stream is encoded with EDGE_MCS6_UL_Encoder, then a normal burst is constructed with EDGE_NormalBurst. Another random bit source is used to simulate the data of the other seven unused time slots. And, a frame is constructed with a Mux2 component. The framed data is modulated and power-controlled with a MpyCx component.
3. The random bit source to simulate the data of the used time slot is delayed one RLC blocks before output because of the delay of the decoder in the receiver.

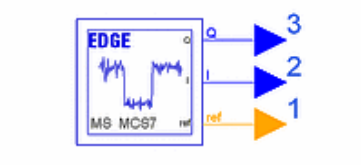


EDGE_MS_MCS6_PwrCtrlSrc Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MS_MCS7_PwrCtrlSrc



Description EDGE signal source for reference sensitivity level test
Library EDGE, Signal Sources
Class SDFEDGE_MS_MCS7_PwrCtrlSrc

Parameters

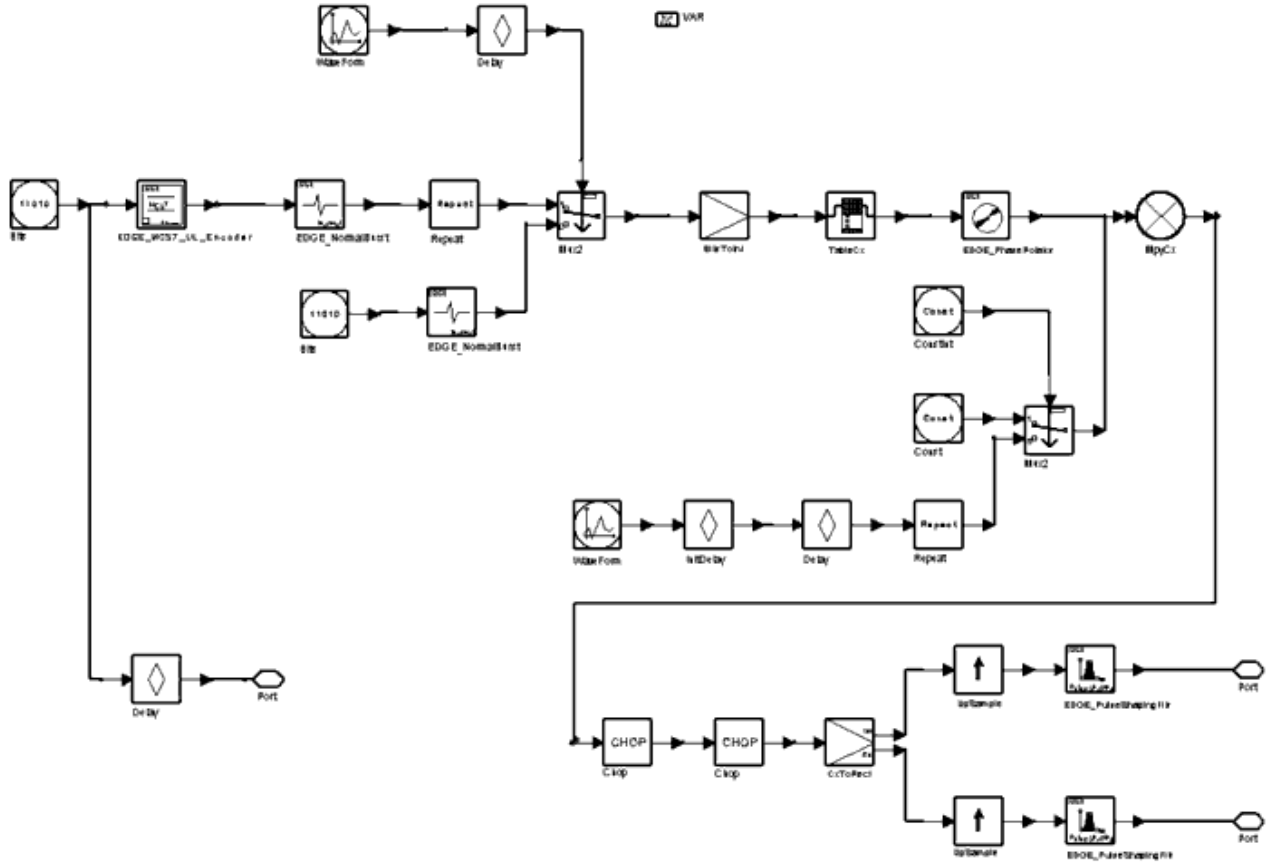
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_Measured	time slot measured	0	int	[0, 7]
TSC	training sequence code	0	int	[0, 7]
PwrState	power control pattern: Power controlled, Full power in each time slot	Power controlled	enum	

Pin Outputs

Pin	Name	Description	Signal Type
1	ref	reference output of bit source with delay adjusted	int
2	I	inphase output	real
3	Q	quadrature output	real

Notes/Equations

1. This subnetwork is used to generate the encoded, framed, modulated and power-controlled downlink EDGE signal for PDTCH/MCS-7.
2. The schematic for this subnetwork is shown in the following figure. A random bit source component is used to simulate the transmitted RLC blocks of the used time slot, and the bit stream is encoded with EDGE_MCS7_UL_Encoder, then a normal burst is constructed with EDGE_NormalBurst. Another random bit source is used to simulate the data of the other seven unused time slots. And a frame is constructed with a Mux2 component. The framed data is modulated and power-controlled with a MpyCx component.
3. The random bit source to simulate the data of the used time slot is delayed one RLC blocks before output because of the delay of the decoder in the receiver. Only data bits is output, the header bits is deleted.

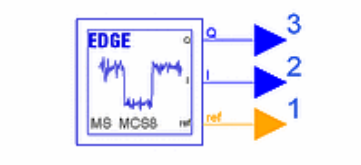


EDGE_MS_MCS7_PwrCtrlSrc Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MS_MCS8_PwrCtrlSrc



Description EDGE signal source for reference sensitivity level test
Library EDGE, Signal Sources
Class SDFEDGE_MS_MCS8_PwrCtrlSrc

Parameters

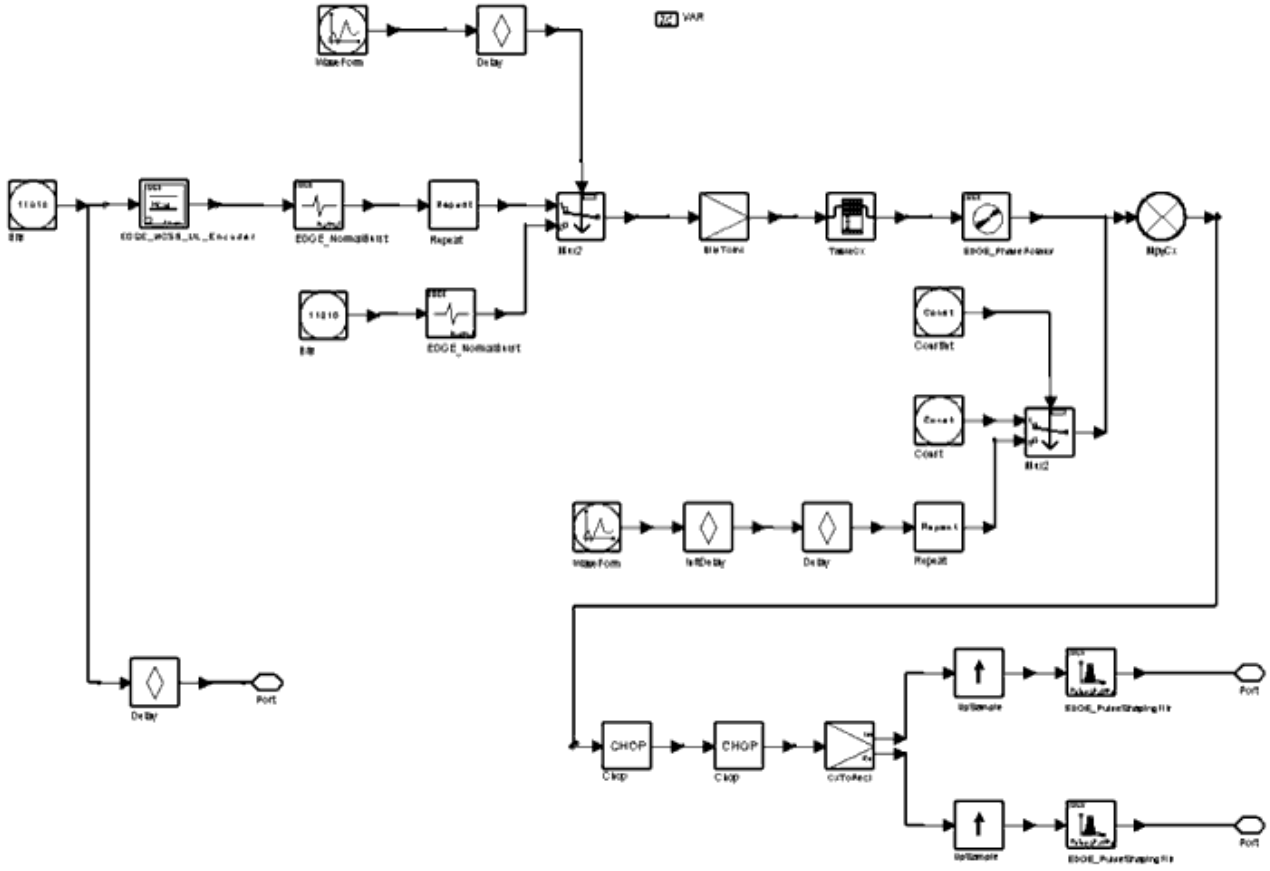
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_Measured	time slot measured	0	int	[0, 7]
TSC	training sequence code	0	int	[0, 7]
PwrState	power control pattern: Power controlled, Full power in each time slot	Power controlled	enum	

Pin Outputs

Pin	Name	Description	Signal Type
1	ref	reference output of bit source with delay adjusted	int
2	I	inphase output	real
3	Q	quadrature output	real

Notes/Equations

1. This subnetwork is used to generate the encoded, framed, modulated and power-controlled downlink EDGE signal for PDTCH/MCS-8.
2. The schematic for this subnetwork is shown in the following figure. A random bit source component is used to simulate the transmitted RLC blocks of the used time slot, and the bit stream is encoded with EDGE_MCS8_UL_Encoder, then a normal burst is constructed with EDGE_NormalBurst. Another random bit source is used to simulate the data of the other seven unused time slots. And a frame is constructed with a Mux2 component. The framed data is modulated and power-controlled with a MpyCx component.
3. The random bit source to simulate the data of the used time slot is delayed one RLC blocks before output because of the delay of the decoder in the receiver. Only data bits is output, the header bits is deleted.

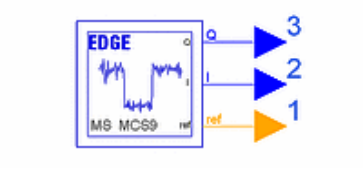


EDGE_MS_MCS8_PwrCtrlSrc Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_MS_MCS9_PwrCtrlSrc



Description EDGE signal source for reference sensitivity level test
Library EDGE, Signal Sources
Class SDFEDGE_MS_MCS9_PwrCtrlSrc

Parameters

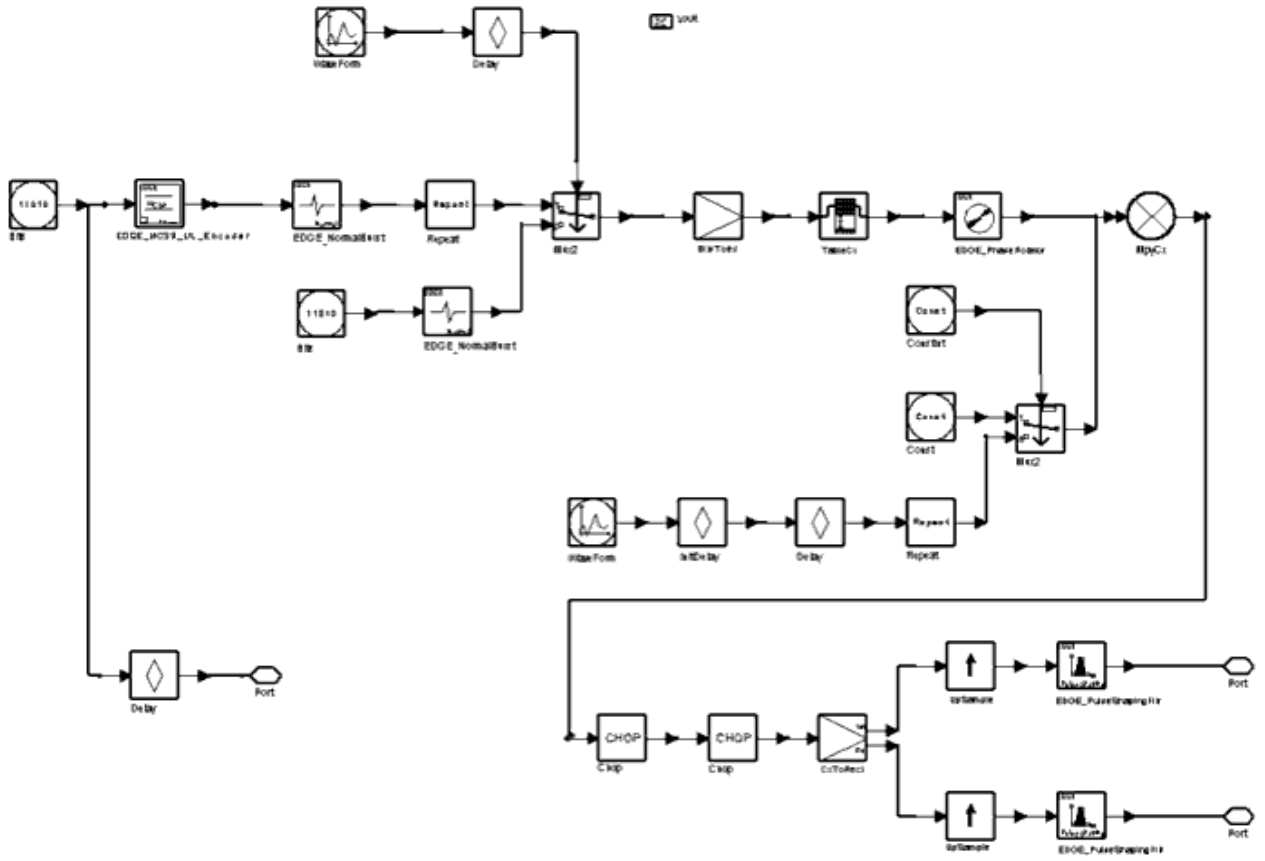
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
TS_Measured	time slot measured	0	int	[0, 7]
TSC	training sequence code	0	int	[0, 7]
PwrState	power control pattern: Power controlled, Full power in each time slot	Power controlled	enum	

Pin Outputs

Pin	Name	Description	Signal Type
1	ref	reference output of bit source with delay adjusted	int
2	I	inphase output	real
3	Q	quadrature output	real

Notes/Equations

1. This subnetwork is used to generate the encoded, framed, modulated and power-controlled downlink EDGE signal for PDTCH/MCS-9.
2. The schematic for this subnetwork is shown in the following figure. A random bit source component is used to simulate the transmitted RLC blocks of the used time slot, and the bit stream is encoded with EDGE_MCS9_UL_Encoder, then a normal burst is constructed with EDGE_NormalBurst. Another random bit source is used to simulate the data of the other seven unused time slots. And a frame is constructed with a Mux2 component. The framed data is modulated and power-controlled with a MpyCx component.
3. The random bit source to simulate the data of the used time slot is delayed one RLC blocks before output because of the delay of the decoder in the receiver. Only data bits is output, the header bits is deleted.

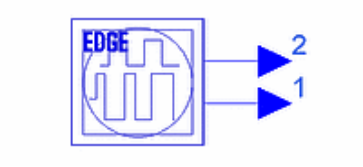


EDGE_MS_MCS9_PwrCtrlSrc Schematic

References

1. ETSI Tdoc SMG2 999/99, CR 05.03-A025 EGPRS Channel Coding, September 20-24, 1999.

EDGE_PatternedSrc



Description EDGE signal source compatible with ESG
Library EDGE, Signal Sources
Class SDFEDGE_PatternedSrc

Parameters

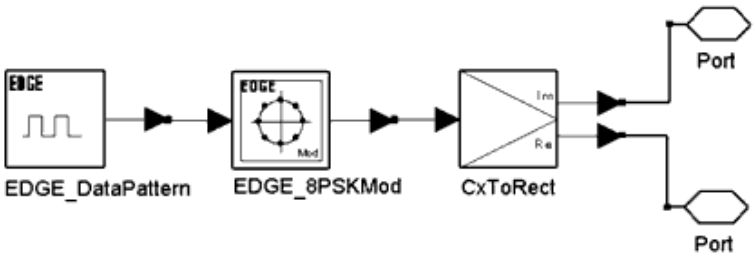
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)
DataPattern	data pattern: PN9, PN15, FIX4, _4_1_4_0, _8_1_8_0, _16_1_16_0, _32_1_32_0, _64_1_64_0	PN9	enum	

Pin Outputs

Pin	Name	Description	Signal Type
1	output_I	inphase output	real
2	output_Q	quadrature output	real

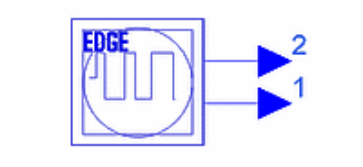
Notes/Equations

1. This subnetwork is used to generate modulated and patterned data.
2. The schematic for this subnetwork is shown in the following figure. EDGE_DataPattern is used to generate one of eight patterned bit streams; the bit stream is 8PSK-modulated; I- and Q-branch modulated data are exported.



EDGE_PatternedSrc Schematic

EDGE_RandomSrc



Description Continuous random data source for EDGE
Library EDGE, Signal Sources
Class SDFEDGE_RandomSrc

Parameters

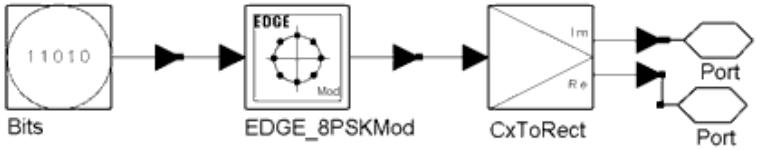
Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	16	int	[1, ∞)

Pin Outputs

Pin	Name	Description	Signal Type
1	I	inphase output	real
2	Q	quadrature output	real

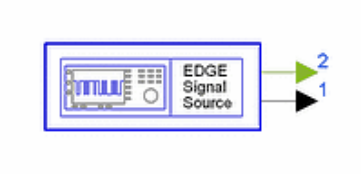
Notes/Equations

1. This subnetwork is used to generate the continuous, random and modulated EDGE signal.
2. The schematic for this subnetwork is shown in the following figure. The component Bits generates random bit stream, and then the data is 8PSK-modulated. The inphase component and quadrature component are output respectively.



EDGE_RandomSrc Schematic

EDGE_Signal_Source



Description VSA compatible signal source
Library EDGE, Signal Sources
Class TSDFEDGE_Signal_Source

Parameters

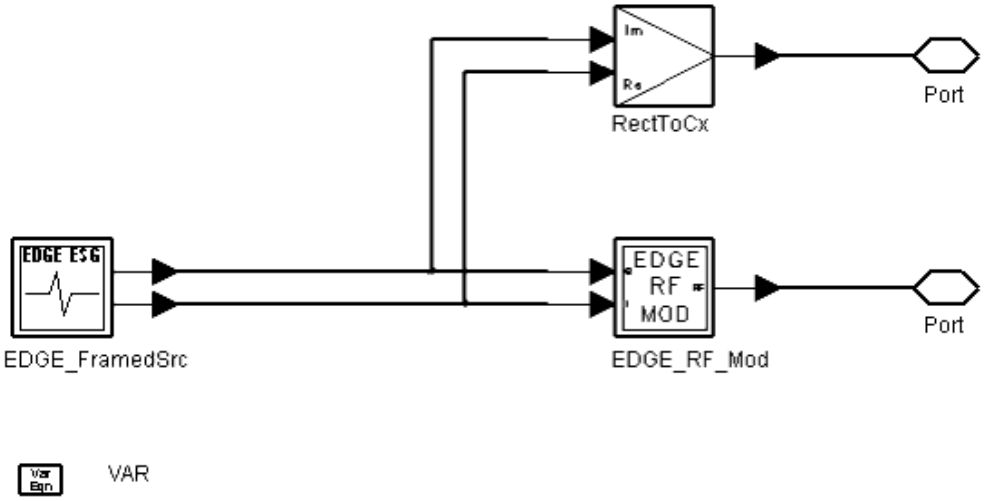
Name	Description	Default	Unit	Type	Range
SampPerSym	number of samples per symbol	8		int	[1, ∞)
TS_State	state of each time slot; 0 for idle, 1 for active	1 1 1 1 1 1 1 1		int array	[0, 1]
DataPattern	data pattern of each time slot: PN9, PN15, FIX4, _4_1_4_0, _8_1_8_0, _16_1_16_0, _32_1_32_0, _64_1_64_0	PN9		enum	
FCarrier	carrier frequency	890.2e6	Hz	real	(0, ∞)
SignalPower	RF signal output power	0.01	W	real	(0, ∞)
PwrType	power on and power off type: None, Linear, Cosine	None		enum	
RampLength	power on and power off length	4		int	[0, 156]
RampUpScramble	scramble of ramp up function	1 1 1 1		real array	(-∞, ∞)
RampDownScramble	scramble of ramp down function	1 1 1 1		real array	(-∞, ∞)
Continues	adding ramp between active slots or not: NO, YES	NO		enum	

Pin Outputs

Pin	Name	Description	Signal Type
1	RF_out	RF output	timed
2	Ref_out	direct output from ESG framed source	complex

Notes/Equations

1. This subnetwork is used to generate framed and modulated EDGE RF or baseband signals. The schematic is shown in the following figure.
   In the output signals, the first and the fifth bursts in one TDMA frame contain 157 symbols, the other bursts contain 156 symbols (as specified in GSM 05.02, version 8.3.0, Release 1999).
2. EDGE_FramedSrc exports patterned, framed and 8PSK-modulated baseband signals at I and Q branches. The baseband signal is moved to a carrier frequency specified by FCarrier and converted to a complex signal before output at Ref_out as the baseband reference signal.

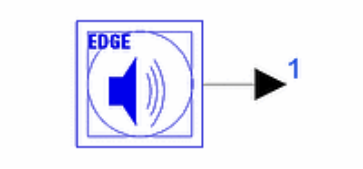


EDGE_Signal_Source Schematic

References

1. CCITT, Recommendation O.151(10/92).
2. CCITT, Recommendation O.153(10/92).
3. GSM 05.02, version 8.3.0, Release 1999.
4. GSM 05.10 for TDMA frame construction.

EDGE_Source



Description EDGE source with framing and modulation
Library EDGE, Signal Sources
Class TSDFEDGE_Source

Parameters

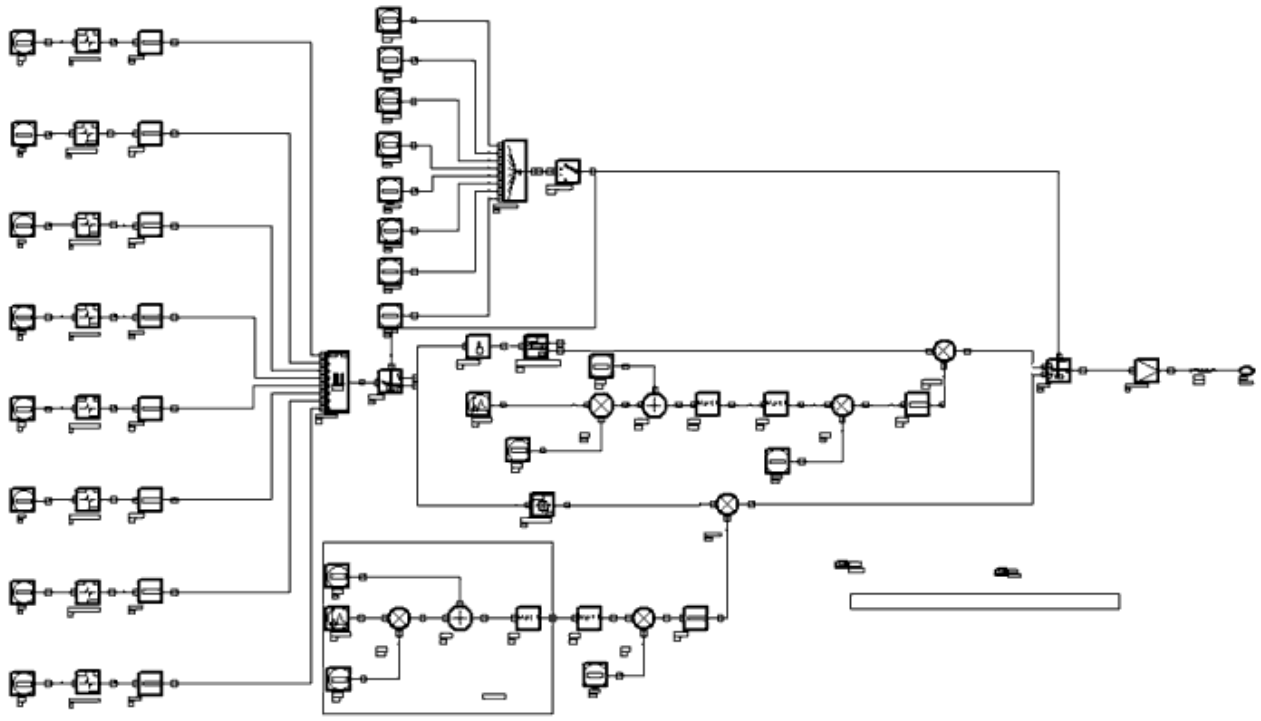
Name	Description	Default	Sym	Unit	Type	Range
SampPerSym	number of samples per symbol: SampleRate 4, SampleRate 8, SampleRate 16	SampleRate 8			enum	[1, ∞)
FCarrier	carrier frequency	935.2 MHz	Fc	Hz	real	[0, ∞)
ModType0	modulation type for time slot 0 (TN0): Modified 8PSK for slot 0, GMSK for slot 0	Modified 8PSK for slot 0			enum	
ModType1	modulation type for time slot 1 (TN1): Modified 8PSK for slot 1, GMSK for slot 1	Modified 8PSK for slot 1			enum	
ModType2	modulation type for time slot 2 (TN2): Modified 8PSK for slot 2, GMSK for slot 2	Modified 8PSK for slot 2			enum	
ModType3	modulation type for time slot 3 (TN3): Modified 8PSK for slot 3, GMSK for slot 3	Modified 8PSK for slot 3			enum	
ModType4	modulation type for time slot 4 (TN4): Modified 8PSK for slot 4, GMSK for slot 4	Modified 8PSK for slot 4			enum	
ModType5	modulation type for time slot 5 (TN5): Modified 8PSK for slot 5, GMSK for slot 5	Modified 8PSK for slot 5			enum	
ModType6	modulation type for time slot 6 (TN6): Modified 8PSK for slot 6, GMSK for slot 6	Modified 8PSK for slot 6			enum	
ModType7	modulation type for time slot 7 (TN7): Modified 8PSK for slot 7, GMSK for slot 7	Modified 8PSK for slot 7			enum	
PowerArray	power of each time slot, in dBm	1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0			real array	
ROut	output resistance	50.0 Ohm		Ohm	real	(0, ∞)

Pin Outputs

Pin	Name	Description	Signal Type
1	output	framed and modulated EDGE data	timed

Notes/Equations

1. This subnetwork is used to generate the framed and modulated EDGE signal. This subnetwork implements both the burst/time slot construction and TDMA framing. The designer can assign 8PSK or GMSK modulation in any time slot with the parameters ModType0 through ModType7. Output signals are timed signals at RF frequency Fc. There are nine modulation and coding schemes (MCS) used in EDGE systems MCS1 through MCS9. MCS1 through MCS4 use GMSK modulation; MCS5 through MCS9 use 8PSK. Different schemes can be chosen for different users according to the channel conditions. So, the different time slots in one TDMA frame may have different modulation schemes, in other words, one TDMA frame may has both the 8PSK and GMSK modulation. This subnetwork can simulate this type of mixed-modulation with the ModType0 to ModType7 parameters.
2. The schematic for this subnetwork is shown in the following figure. Eight random bit source components are used to simulate the data of eight users that are in the same TDMA frame. A normal burst for each user is constructed by adding the training sequence, tail bits, guard bits and stealing flag bits to the user data. Since one 8PSK modulated symbol corresponds to three bits, each bit in the GMSK modulated slots is repeated three times to make all the slots have the same length. This is because that the demultiplexer DeMux2 can only split data into blocks of the same size.
   Going through the DeMux2, data is split into two paths, the upper path for GMSK modulation and the lower path for 8PSK. Before GMSK modulation, input bits are down-sampled by a 1/3 rate, which is the reverse process of the repeat. ModType0 to ModType7 determine the modulation type of each time slot in each frame.
   PowerArray controls the output signal power of each time slot. The power control is implemented at the multiplier MpyCx2 (M8 and M2). The branches connected in at the multipliers carry the gain factors that are based on the PowerArray and then calibrated in the branches. The framed and modulated complex symbols are then transformed into the timed data using the carrier frequency defined by FCarrier.



EDGE_Source Schematic

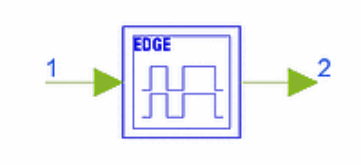
References

1. ETSI Tdoc SMG2 WPB 108/98, Ericsson, EDGE Evaluation of 8-PSK.
2. ETSI Tdoc SMG2 EDGE 130/99, Ericsson, EDGE: Concept Proposal for Enhanced GPRS, May 17 -19, 1999.

Synchronization Components for EDGE Design Library

- *EDGE BitSync* (edge)
- *EDGE DownSample* (edge)
- *EDGE ESG Sync* (edge)
- *EDGE PhaseRecovery* (edge)
- *EDGE SymbolPrecede* (edge)
- *EDGE TrainBitGen* (edge)

EDGE_BitSync



Description Bit synchronization for 8PSK modulated bursts
Library EDGE, Synchronization
Class SDFEDGE_BitSync

Parameters

Name	Description	Default	Type	Range
BurstType	burst type: Normal Burst, Synchronization Burst, Access Burst	Normal Burst	enum	
SampPerSym	number of samples per symbol	8	int	(0, ∞)
TSC	training sequence code	0	int	[0, 7] for Normal Burst

Pin Inputs

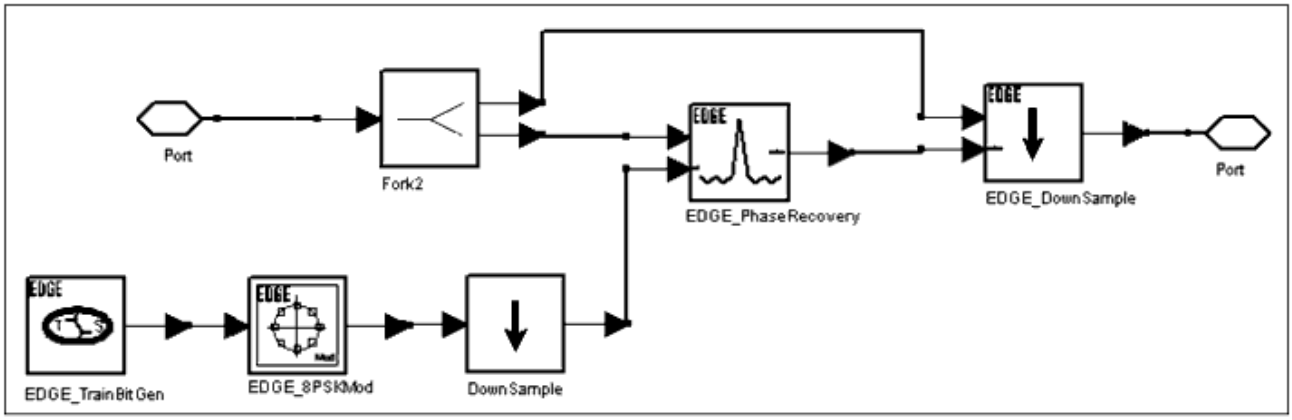
Pin	Name	Description	Signal Type
1	input	input signal to be bit synchronized	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	output	bit synchronized and down-sampled data	complex

Notes/Equations

1. This subnetwork implements bit synchronization for 8PSK modulated signals.
2. The schematic for this subnetwork is shown in the following figure. It consists of a training sequence generator, an 8-PSK modulator, phase recovery, and a downsampler.
   The training sequence used in framing is generated and modulated locally. The phase recovery model detects the time delay and optimum phase by calculating the correlation between the input signal and local modulated training sequence. The downsampler EDGE_DownSample decimates the input signal using the input index from EDGE_PhaseRecovery.

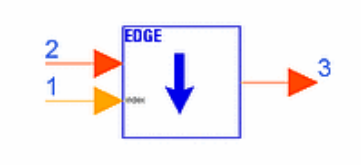


EDGE_BitSync Schematic

References

1. G. D'Aria and F. Muratore, and V. Palestini, "Simulation and Performance of the Pan-European Land Mobile Radio System," IEEE Trans. Veh. Technol., Vol. 41, pp. 177-189, May 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, addressing and identification, version 3.5.1, March 1992.
4. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, *Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities* , version 3.5.1, March 1992.
5. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999

EDGE_DownSample



Description EDGE burst down-sample
Library EDGE, Synchronization
Class SDFEDGE_DownSample

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8	N	int	(0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	index	index of sample point to be output	int
2	input	oversampled data	anytype

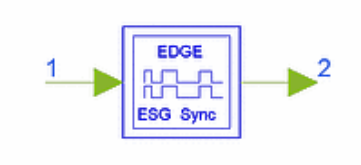
Pin Outputs

Pin	Name	Description	Signal Type
3	output	synchronized data	anytype

Notes/Equations

1. This model is used to down-sample the input over-sampled EDGE burst using the index detected by EDGE_PhaseRecovery.
   Each firing, 156 tokens are produced at output when 156 × N tokens are consumed at input and one token is consumed at index, where N is the number of samples per symbol.
2. This model decimates the input over-sampled EDGE burst with rate of N starting from the index input. 0s are added to the tail of the output to form an EDGE burst of 156 symbols.

EDGE_ESG_Sync



Description Synchronization for ESG
Library EDGE, Synchronization
Class SDFEDGE_ESG_Sync

Parameters

Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)

Pin Inputs

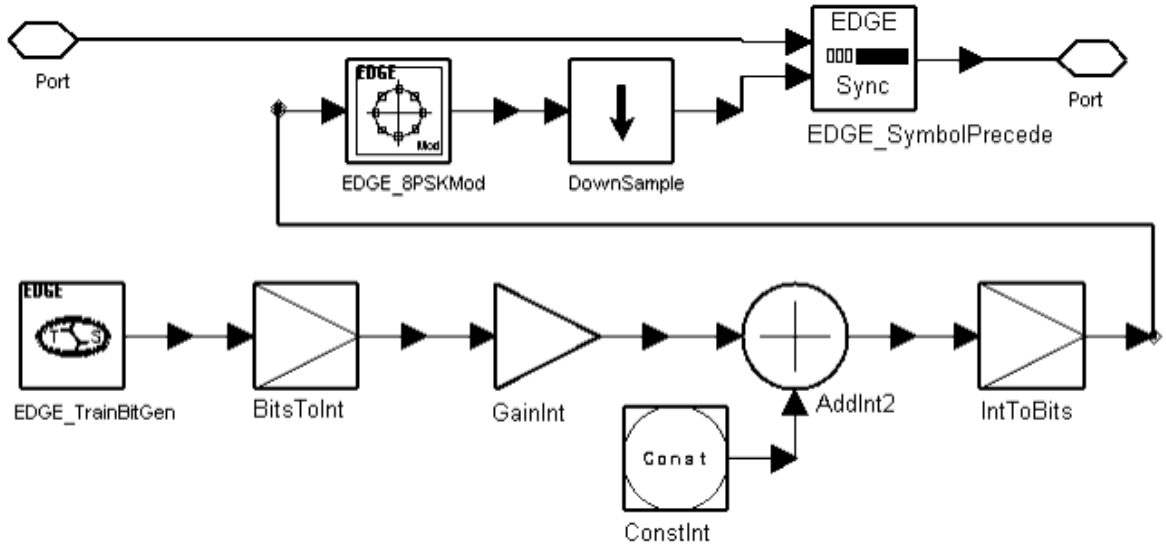
Pin	Name	Description	Signal Type
1	input	modulated data to be synchronized	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	output	correct content of a frame	complex

Notes/Equations

1. This subnetwork implements bit synchronization for 8PSK modulated signals for ValiFire.
   Each firing, 1250 × SampPerSym tokens representing samples of a modulated frame are consumed at the input; 1250 × SampPerSym tokens representing a synchronized frame are generated.
   - if SampPerSym = 2, 2500 tokens will be input and output
   - if SampPerSym = 4 or 8, 5000 or 10000 tokens, respectively, will be input and output
2. The schematic for this subnetwork is shown in the following figure. It consists of a training sequence generator, an 8PSK modulator, a downsampler, and a synchronizer. The training sequence used in framing is generated and modulated locally.
   The synchronizer determines the time delay and optimum phase in the first frame by correlating the input signal and local modulated training sequence; From the second frame on, it will output the correct frame streams without a delay using the index position derived from first frame.



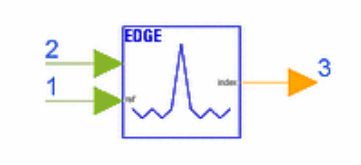
EDGE_ESG_Sync Schematic

References

1. G. D'Aria and F. Muratore, and V. Palestini, "Simulation and Performance of the Pan-European Land Mobile Radio System," IEEE Trans. Veh. Technol., Vol. 41, pp. 177-189, May 1992.

2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, addressing and identification, version 3.5.1, March 1992.
4. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities, version 3.5.1, March 1992.
5. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999.

EDGE_PhaseRecovery



Description Index of sequence with peak correlation value
Library EDGE, Synchronization
Class SDFEDGE_PhaseRecovery

Parameters

Name	Description	Default	Sym	Type	Range
SampPerSym	number of samples per symbol	8	N	int	(0, ∞)
BurstType	burst type: Normal Burst, Synchronization Burst, Access Burst	Normal Burst		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	ref	reference local data	complex
2	input	data to be synchronized	complex

Pin Outputs

Pin	Name	Description	Signal Type
3	index	index of sampling data	int

Notes/Equations

1. This model is used to implement correlation between the received modulated training sequence and the local modulated training sequence to estimate the timing offset and detect the optimum phase.
   Each firing, one token is produced at index when 156 × N tokens are consumed at input and M tokens are consumed at ref, where N is the number of samples per symbol and M is the number of modulated training sequence symbols in a burst. Refer to the following table for M values.

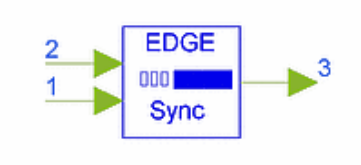
BurstType	M
Normal Burst	26
Synchronization Burst	64
Access Burst	41

2. This model detects the time delay and optimum phase by calculating the correlation between input signal and local modulated training sequence. The length of the slide correlation window equals the guard period. Thus, the maximum delay that can be detected is the guard period. When the delay is no less than the guard period, a warning message will appear.

References

1. G. D'Aria and F. Muratore, and V. Palestini, "Simulation and Performance of the Pan-European Land Mobile Radio System," IEEE Trans. Veh. Technol., Vol. 41, pp. 177-189, May 1992.

EDGE_SymbolPrecede



Description Output the correct content of a frame
Library EDGE, Synchronization
Class SDFEDGE_SymbolPrecede

Parameters

Name	Description	Default	Type	Range
SampPerSym	number of samples per symbol	8	int	[1, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	ref	reference local data	complex
2	input	data to be synchronized	complex

Pin Outputs

Pin	Name	Description	Signal Type
3	output	correct content of a frame	complex

Notes/Equations

This model implements an internal correlation function between local modulated training sequence symbols and input modulated samples.

Delays introduced by pulse-shaping filters are calculated in the first frame, where samples will be padded with 0s as necessary; from the second and subsequent frames, the correct frame streams will be output without a delay using the index position derived from first frame.

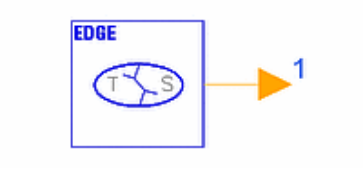
Each firing, 26 tokens representing the local modulated training sequence are consumed at ref pin 1; 1250 × SampPerSym tokens representing samples of a modulated frame to be synchronized are consumed at input pin 2. 1250 × SampPerSym tokens representing a synchronized frame are output.

- if SampPerSym = 2, 2500 tokens will be input at pin 2 and output
- if SampPerSym = 4 or 8, 5000 or 10000 tokens, respectively, will be input and output

References

1. G. D'Aria and F. Muratore, and V. Palestini, "Simulation and Performance of the Pan-European Land Mobile Radio System," IEEE Trans. Veh. Technol., Vol. 41, pp. 177-189, May 1992.

EDGE_TrainBitGen



Description Training bits generation
Library EDGE, Synchronization
Class SDFEDGE_TrainBitGen

Parameters

Name	Description	Default	Type	Range
ModType	modulation type: Modified 8PSK, GMSK	Modified 8PSK	enum	
BurstType	burst type: Normal Burst, Synchronization Burst, Access Burst	Normal Burst	enum	
TSC	training sequence code	0	int	[0, 7] for Normal Burst

Pin Outputs

Pin	Name	Description	Signal Type
1	output	training sequence	int

Notes/Equations

1. This model is used to generate training sequences.
   The following table lists the output token values.

Burst Type	Modified 8PSK Output Tokens	GMSK Output Tokens
Normal Burst	26×3	26
Access Burst	41×3	41
Synchronization Burst	64×3	64

2. The first of the following two tables shows the relationship between TSC and Training Sequences Bits for Normal Burst defined in GSM 05.02 standard. The model outputs the corresponding training sequence according to the TSC parameter. TSC is ignored when BurstType is set to Synchronization Burst.
   Synchronization Burst synchronization sequence is:

   {1,0,1,1,1,0,0,1,0,1,1,0,0,0,1,0,0,0,0,0,0,1,0,0,0,0,0,0,1,1,1,1,0,0,1,0,1,1,0,1,
   0,1,0,0,0,1,0,1,0,1, 1,1,0,1,1,0,0,0,0,1,1,0,1,1}

   In EDGE, two new training sequences are introduced. The relationship between TSC and training sequence bits for access burst is listed in the second of the following two tables.
   In EDGE system, the same training sequences as defined for GSM are used, by using the BPSK subset of the 8PSK symbol constellation during the midamble [4]. Thus, when ModType is set to Modified 8PSK, each bit of the training sequence selected is mapped into three bits with `0' to `001' and `1' to `111' before being output.
   When ModType is set to GMSK, one of the training sequences described above is output directly.

TSC	Training Sequences
0	0,0,1,0,0,1,0,1,1,1,0,0,0,0,1,0,0,0,1,0,0,1,0,1,1,1
1	0,0,1,0,1,1,0,1,1,1,0,1,1,1,1,0,0,0,1,0,1,1,0,1,1,1
2	0,1,0,0,0,0,1,1,1,0,1,1,1,0,1,0,0,1,0,0,0,0,1,1,1,0
3	0,1,0,0,0,1,1,1,1,0,1,1,0,1,0,0,0,1,0,0,0,1,1,1,1,0
4	0,0,0,1,1,0,1,0,1,1,1,0,0,1,0,0,0,0,0,0,1,1,0,1,0,1,1
5	0,1,0,0,1,1,1,0,1,0,1,1,0,0,0,0,0,0,1,1,0,0,1,1,1,0,1,0
6	1,0,1,0,0,1,1,1,1,1,0,1,1,0,0,0,1,0,1,0,0,1,1,1,1,1
7	1,1,1,0,1,1,1,1,0,0,0,1,0,0,1,0,1,1,1,0,1,1,1,1,0,0

TSC	Training Sequence Bits
0	0,1,0,0,1,0,1,1,0,1,1,1,1,1,1,1,1,0,0,1,1,0,0,1,1,0,1,0,1,0,1,0,0,0,1,1,1,1,0,0,0
1	0,1,0,1,0,1,0,0,1,1,1,1,1,0,0,0,1,0,0,0,0,1,1,0,0,0,1,0,1,1,1,1,0,0,1,0,0,1,1,0,1
2	1,1,1,0,1,1,1,1,0,0,1,0,0,1,1,1,0,1,0,1,0,1,1,0,0,0,0,0,1,1,0,1,1,0,1,1,1,0,1,1,1

References

1. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.02, Multiplexing and Multiple Access on the Radio Path, version 3.5.1, March 1992.
2. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 03.03, Numbering, addressing and identification, version 3.5.1, March 1992.
3. European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 04.03, *Mobile Station - Base Station System (MS - BSS) Interface Channel Structures and Access Capabilities* , version 3.5.1, March 1992.
4. Tdoc SMG2 EDGE 130/99, EDGE: Concept Proposal for Enhanced GPRS, Ericsson, p. 13, May 17 - 19, 1999
5. Tdoc SMG2 EDGE 2E99-403, EDGE: New Training Sequences for Access Burst due to EGPRS,SMG2EDGE WS #10, August 24 - 27, 1999.